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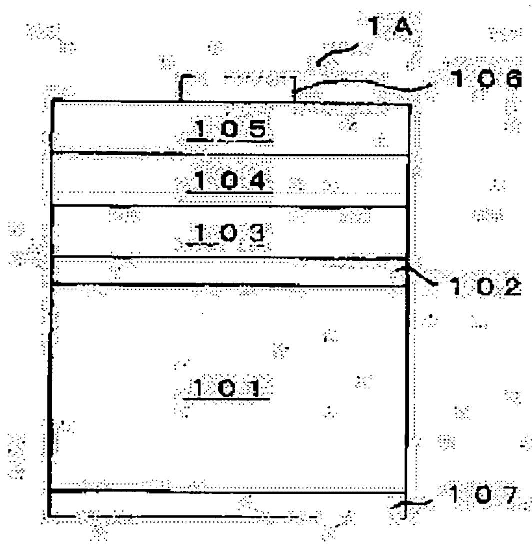
(54) LAYERED STRUCTURAL UNIT, ITS MANUFACTURING METHOD, LIGHT EMITTING DEVICE, LAMP, AND LIGHT SOURCE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a high quality crystal layer within a temperature range much wider than that obtained by a conventional constitution, to form a boron phosphite system semiconductor layer which comprises a crystal surface having a constant surface index without depending upon a surface index of a substrate surface and is formed so as to have the surface index agree with a direction showing clear cleavage, and to make a layered structural unit from the boron phosphite system semiconductor layer.
SOLUTION: After a buffer layer made of amorphous or polycrystalline boron phosphite system semiconductor is formed on a semiconductor substrate, a {110}-boron phosphite system semiconductor crystal layer is formed within a temperature range of 750° C-1200° C on the buffer layer.



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CLAIMS

[Claim(s)]
[Claim 1] The laminating structure characterized by providing the Lynn-ized boron system semiconducting crystal layer (it being called a {110}-Lynn-ized boron system semiconducting crystal layer.) to which it comes to carry out the laminating of the crystal face which sets to {110} the indices of crystal plane of a front face parallel to the front face of a single crystal substrate prepared on the single crystal substrate, the buffer coat which consists of an amorphous substance prepared in the front face of this single crystal substrate, or a Lynn-ized boron system semi-conductor of polycrystal, and this buffer coat.
[Claim 2] The laminating structure according to claim 1 characterized by preparing the {110}-Lynn-ized boron system semiconducting crystal layer on the front face of the cubic single crystal substrate which sets indices of crystal plane to {100}.
[Claim 3] The laminating structure according to claim 1 characterized by preparing the {110}-Lynn-ized boron system semiconducting crystal layer on the front face of the cubic single crystal substrate which sets indices of crystal plane to {111}.
[Claim 4] The laminating structure given in claim 1 characterized by consisting of Lynn-ized boron system semi-conductors of the polycrystal with which the buffer coat prepared on the single crystal substrate includes the crystal face which carries out indices of crystal plane except {110} thru/or any 1 term of 3.
[Claim 5] The laminating structure according to claim 4 characterized by consisting of Lynn-ized boron system semi-conductors of the polycrystal with which the buffer coat prepared on the single crystal substrate includes the crystal face which sets indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is a positive integer).
[Claim 6] The laminating structure given in claim 1 characterized by consisting of ingredients with which a {110}-Lynn-ized boron system semiconducting crystal layer contains the Lynn-ized boron (boron monophosphide) of the monomer which makes the band gap in a room temperature 3.0**0.2 electron volts (eV) thru/or any 1 term of 5.
[Claim 7] The manufacture approach of the laminating structure given in claim 1 characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on a single crystal substrate thru/or any 1 term of 6.
[Claim 8] The manufacture approach of the laminating structure according to claim 7 characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on the single crystal substrate which makes a front face the {100} crystal faces.
[Claim 9] The manufacture approach of the laminating structure according to claim 7 characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on the single crystal substrate which makes a front face the {111} crystal faces.
[Claim 10] The manufacture approach of the laminating structure given in claim 7 characterized by forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at low temperature rather than a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 9.
[Claim 11] The manufacture approach of the laminating structure given in claim 7 characterized by forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at 250-degree-C or more temperature of 700 degrees C or less thru/or any 1 term of 10.
[Claim 12] After forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at 250-degree-C or more temperature of 700 degrees C or less, it heat-treats to a buffer coat at an elevated temperature more. The manufacture approach of the laminating structure given in claim 7 characterized by forming the buffer coat which consists of a Lynn-ized boron system semi-conductor of the polycrystal which has the crystal face which sets indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is a positive integer) thru/or any 1 term of 11.

[Claim 13] The light emitting device using the laminating structure given in claim 1 possessing the buffer coat which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 6.
[Claim 14] The light emitting device using the laminating structure given in claim 1 possessing the barrier layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 6.
[Claim 15] The light emitting device using the laminating structure given in claim 1 possessing the current inhibition (constriction) layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 6.
[Claim 16] The light emitting device using the laminating structure given in claim 1 possessing the electrode contact layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 6.
[Claim 17] The light emitting device using the laminating structure given in claim 1 possessing the semi-conductor multilayers reflecting mirror with which at least a part consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or any 1 term of 6.
[Claim 18] The lamp using a light emitting device given in claim 13 thru/or any 1 term of 17.
[Claim 19] The light source using a lamp according to claim 18.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the laminating structure equipped with the Lynn-ized boron (BP) system semiconducting crystal layer which has the front face of indices of crystal plane which is different from the indices of crystal plane of a single crystal substrate front face, and its manufacture approach. Moreover, it is related with the light emitting device, the lamp, or the light source produced from the laminating structure.
[0002]
[Description of the Prior Art] As for Lynn-ized boron (BP), ionicity has with 0.006 the description from which it can be easy to obtain the semi-conductor layer of low (refer to the Philips work, a "semi-conductor joint theory" (Yoshioka Shoten, July 25, 1985 issue, the 3rd **), and 49 - 51 pages) especially p form conductivity. The property of such Lynn-ized boron (BP) acts for constituting the light-emitting part of a pn junction mold simple at dominance. For this reason, the technique which constitutes light emitting devices, such as light emitting diode (LED) or a laser diode (LD), from the laminating structure equipped with the Lynn-ized boron system group-III-V-semiconducter layer is indicated from the former (refer to JP,2-288388,A). In the former, the laminating structure of a light emitting device application is constituted considering group-III-V-semiconducter single crystals, such as gallium phosphide (GaP) and gallium nitride (GaN), as a substrate (refer to ** JP,2-275682,A and ** JP,10-247745,A each official report). Moreover, the silicon (Si) single crystal (silicon) is known as another substrate ingredient (refer to U.S. Pat. No. 6,069,021 number). Moreover, silicon carbide (SiC) is also used as a substrate ingredient (refer to patent No. 2,809,690).
[0003] In the former, the Lynn-ized boron system semi-conductor layer is used as various stratum functionale. For example, the green laser diode (LD) of the current constriction mold equipped with the Lynn-ized boron (BP) layer as a current blocking layer is indicated by invention given in JP,10-242569,A. Moreover, there is also a well-known example which makes the laminating structure possess the Lynn-ized boron (BP) layer as a contact (contact) layer for forming an ohmic (Ohmic) electrode (refer to JP,10-242568,A). Moreover, the light emitting diode (LED) equipped with the Lynn-ized boron (BP) layer as a buffer coat is also well-known (refer to JP,10-242514,A). In order to ease better the lattice mismatch (mismatch) of a substrate ingredient and a laminating structure configuration layer especially, the example which constitutes the so-called low-temperature buffer coat formed at low temperature in comparison from a Lynn-ized boron (BP) system semi-conductor layer is known (refer to the above-mentioned U.S. Pat. No. 6,069,021 number). For example, the technique which constitutes a buffer coat from gallium phosphide and boron (BXGa1-XP:0 <=X<=1) on silicon or a gallium phosphide (GaP) single crystal substrate is indicated (refer to JP,11-266006,A).

[0004] On the other hand, when silicon is used as a substrate, the temperature as which the Lynn-ized boron (BP) layer of a single crystal is concluded is limited to the very narrow range of 1020 degrees C - 1070 degrees C and at most 50 degrees C (refer to the Nishinaga **, "application physics", volume [45th] No. 9 (1976), and 891 - 897 pages). Only in this narrow temperature requirement, it is supposed that a Lynn-ized boron (BP) single crystal layer is obtained, and it is supposed that it is a polycrystal layer the Lynn-ized boron layer obtained at other low temperature or another elevated temperature (refer to the above-mentioned "application physics" and the 45th volume). moreover, a (100)-gallium phosphide (GaP) single crystal -- a substrate -- carrying out -- diboron hexahydride (B-2 H6) / phosphine (PH3) / hydrogen (H2) system-of-reaction organic metal pyrolysis vapor growth (MOCVD) -- it depends on law and there is also the conventional example which formed the Lynn-ized boron (BP) layer at 1150 degrees C (refer to Inst.Phys.Conf.Ser., No.129 (IOP Publishing Ltd., 1993), and Chapter 3,157-162 pages). Even in this case, the Lynn-ized boron (BP) layer obtained is the so-called polycrystal layer in which the crystal face (100) and the other crystal face are intermingled (the Inst.Phys.Conf.Ser.No.129 above-mentioned reference).
[0005] When a cubic single crystal is used as a substrate, the indices of crystal plane of the Lynn-ized boron (BP) single crystal layer formed only in a very narrow temperature requirement are not dependent on a growth means, and are made the same as that of the indices of crystal plane on the front face of a substrate. For example, in halogen (halogen) vapor growth, the Lynn-ized boron (BP) single crystal layer which similarly sets indices of crystal plane to (111) is formed on the silicon substrate which sets indices of crystal plane to (111) (J. refer to Crystal Growth.13 / 14 (1972) or 346 pages). moreover, MOCVD -- law -- indices of crystal plane -- or (100) (110) -- ** -- it is supposed that the Lynn-ized boron (boron monophosphide) of the monomer of

the same indices of crystal plane is too formed on the front face of the silicon substrate to carry out (it is in Jpn.J.Appl.Phys., 13 (3) and (1974), and 411-416 pages, and see the 413 pages especially). That is, in the former, what can be used for, for example, constituting the laminating structure of a light emitting device application was the Lynn-ized boron (BP) crystal layer which grew with the same indices of crystal plane as the indices of crystal plane on the front face of a substrate (the Shono Katsufusa work, "semiconductor technology (above)" (refer to University of Tokyo Press and June 25, 1992 issue 9 **, 77 pages, and 99 pages).).

[0006] Moreover, about Lynn-ized boron (BP), various band gaps are reported from the former. For example, B.Stone and others has got the room temperature band gap of about 6 electron volts (eV) from the polycrystal BP film (Phys.Rev.Lett., Vol.4, No.6 (1960), 282-284-page **). Moreover, if it depends on Manca, the 4.2eV band gap is shown (J. refer to Phys.Chem.Solids, 20 (1961), and 268.). Moreover, it is supposed that it is the band gap of Lynn-ized boron about 2eV (refer to **RCA Review, 25 (1964), 159-167 pages and **Z.anorg.allg.chem., 349 (1967), and 151-157 pages). In the present condition, the band gap in the room temperature of Lynn-ized boron (BP) is accepted noting that it is about 2eV (the Teramoto ****, "semiconductor device introduction" (refer to Baifukan Co., Ltd., the March 30, 1995 issue first edition, and 28 pages).). For this reason, the semi-conductor property of the Lynn-ized boron (BP) system mixed crystal used for constituting the laminating structure of an LED application is designed considering the room temperature band gap of BP as 2eV (refer to JP,2-275682,A and JP,10-247760,A each official report).

[0007] The technique which forms BP system mixed-crystal object of a higher band gap is also indicated using about 2eV Lynn-ized boron (BP). For example, the 2.7eV band gap has been obtained from the superstructure of the alumimium nitride gallium mixed-crystal (Ga0.5aluminum0.5N) thin layer (thickness = 1nm) of undoping (undope), and the Lynn-ized boron (BP) thin layer (thickness = 1nm) (refer to JP,10-247745,A). Moreover, the 3.0eV band gap has been obtained from the superstructure of a Ga0.5aluminum0.5N thin layer (thickness = 1.3nm) and the Lynn-ized boron (BP) thin layer (thickness = 0.7nm) (refer to JP,2-288371,A). Or the Lynn-ized boron system mixed crystal of a high band gap is obtained by considering as plural mixed crystal using Lynn-ized boron (BP) (refer to above-mentioned JP,2-288371,A). For example, the semi-conductor layer which sets the band gap of the 0.3B0.4N0.6P 0.45 yuan of Ga0.3aluminum to 3eV as mixed crystal has been obtained (refer to above-mentioned JP,2-288371,A). Moreover, for example, the semi-conductor layer which sets the band gap of the 0.25B0.50N0.60P 0.405 yuan of Ga0.25aluminum to 2.7eV as mixed crystal has been obtained (refer to above-mentioned JP,2-288371,A).

[0008]

[Problem(s) to be Solved by the Invention] When a cubic single crystal is used as a substrate so that the above-mentioned Prior art may teach, the temperature requirement which can obtain the Lynn-ized boron (BP) system semi-conductor layer of the single crystal which has the same indices of crystal plane as a substrate is very narrow. Now, simple, it is stabilized and the laminating structure equipped with the Lynn-ized boron (BP) system semi-conductor layer cannot be formed. the hexagonal (hexagonal) silicon carbide (a-axis lattice constant **3.08A) with which the temperature requirement which can be concluded in the Lynn-ized boron layer of a single crystal makes smallness a difference with the spacing (**3.21A) between the crystal faces (111) of Lynn-ized boron (lattice constant **4.54A) -- a substrate -- then, it is supposed that it can widen (refer to the above-mentioned "application physics", the 45th volume, and 894 pages). The temperature from which the Lynn-ized boron layer of a single crystal is obtained becomes 1050 degrees C - 1150 degrees C, and it is reported that the range can be widened to 100 degrees C (J. refer to Appl.Phys., 42 (1) and (1971), and 420 - 424 pages).

[0009] Moreover, the indices of crystal plane of the Lynn-ized boron layer are (111) to (0001) of a hexagonal substrate (above-mentioned J.Appl.Phys., 42 (1971) reference). The Lynn-ized boron (boron monophosphide) of a monomer is a cube zinc sulfide ore type (spharelite) (refer to the above-mentioned "semi-conductor joint theory" and 14 - 15 pages) crystal, and has clear cleavability in the [110] directions. Cleavage is not easy in the Lynn-ized boron crystal layer in which the crystal layer which the above-mentioned hexagonal silicon carbide presents clear cleavability, and is not upwards and sets indices of crystal plane to (111) carried out the laminating. It does not come to constitute the laser diode which follows, for example, uses a cleavage plane as a resonance side simple.

[0010] Moreover, in the conventional technique, since BP system semi-conductor layer constitutes BP which makes a band gap low with about 2eV as a parent ingredient, it did not come to obtain BP system mixed-crystal layer equipped with sufficient high prohibition width of face to penetrate luminescence of short wavelength. When giving an example, there was a fault in which the BXGa1-XP (0<=X<=1) mixed-crystal layer which sets a band gap to about 2.3eV at the maximum is formed and over which it does not pass from BP and GaP (band gap **2.3eV) which set a band gap to 2.0eV. Now, since short wavelength luminescence of a purple-blue color etc. will be absorbed, the problem to which LED of high brightness which is excellent in the drawing effectiveness of luminescence to the exterior is not brought had arisen from the Lynn-ized boron system semi-conductor preparation ****** structure of such a low band gap, for example.

[0011] With the conventional technique for on the other hand obtaining the semi-conductor layer of a higher band gap using the Lynn-ized boron (BP) which sets a band gap to about 2eV, the laminating of the about several nm ultra-thin film must be carried out by turns periodically, and it must consider as a superstructure, and in order to stabilize and control a presentation in the thickness list of the ultra-thin film, complicated and

redundant membrane formation actuation is needed. Moreover, the special membrane formation equipment for forming a superstructure is also demanded (refer to above-mentioned JP,2-288371,A). Furthermore, it is difficult to maintain the presentation of the configuration element of mixed crystal to stability with the conventional technique of forming the mixed crystal of 5 yuan (five elements) originally, using the small Lynn-ized boron (BP) of a band gap, and obtaining the Lynn-ized boron (BP) system mixed-crystal layer of a higher band gap. In formation of mixed crystal, the number of configuration elements is increased, and common knowledge already becomes difficult [stable membrane formation], so that it is plural mixed crystal (refer to the above-mentioned "semiconductor device introduction" and 24 pages). It is stabilized, and it can form and aluminum-arsenide gallium (AlXGa1-XAs:0 <=X<=1) the mixed crystal of 3 yuan, and aluminium phosphide gallium indium (AlXGa1-X) (YIn1-YP:0 <=X<=1, 0<=Y<=1) the mixed crystal of 4 yuan are used (refer to the above-mentioned "semiconductor device introduction" and 24 pages).

[0012] what was made that this invention should conquer the trouble of the above-mentioned conventional technique -- it is -- (**) -- being possible in there being nothing to the former and obtaining a good crystal layer in a large temperature requirement -- accomplishing -- (**) -- the ** independent of the indices of crystal plane on the front face of a substrate -- from the crystal face of fixed indices of crystal plane -- becoming -- in addition -- and (Ha) the technique for constituting the laminating structure from a Lynn-ized boron system semi-conductor layer formed so that it might agree in the direction in which the indices of crystal plane present clear cleavage shows. moreover, (**) -- the manufacture approach which is forming the laminating structure possessing the Lynn-ized boron system semi-conductor layer which has the description of a publication in a **** (Ha) term with dominance is offered. Furthermore, it is making into the meaning to offer the light emitting device which is excellent in the luminescence property produced from the laminating structure, the lamp (lamp) which used it for the list, and the light source.

[0013]

[Means for Solving the Problem] That is, this invention is the laminating structure equipped with the Lynn-ized boron system semi-conductor layer which carried out the laminating on the substrate of a single crystal, and is the laminating structure which equipped (following 1) thru/or following (6) terms with the description of a publication.

(1) The laminating structure characterized by to provide the Lynn-ized boron system semiconducting crystal layer (for it to be called a {110}-Lynn-ized boron system semiconducting crystal layer.) to which it comes to carry out the laminating of the crystal face which sets to {110} the indices of crystal plane of a front face parallel to the front face of a single crystal substrate prepared on the single crystal substrate, the buffer coat which consists of an amorphous substance prepared in the front face of this single crystal substrate, or a Lynn-ized boron system semi-conductor of polycrystal, and this buffer coat.

(2) The laminating structure given in the above (1) characterized by preparing the {110}-Lynn-ized boron system semiconducting crystal layer on the front face of the cubic single crystal substrate which sets indices of crystal plane to {100}.

(3) The laminating structure given in the above (1) characterized by preparing the {110}-Lynn-ized boron system semiconducting crystal layer on the front face of the cubic single crystal substrate which sets indices of crystal plane to {111}.

(4) The above (1) characterized by consisting of Lynn-ized boron system semi-conductors of the polycrystal with which the buffer coat prepared on the single crystal substrate includes the crystal face which carries out indices of crystal plane except {110} thru/or the laminating structure given in any 1 term of (3).

(5) The laminating structure given in the above (4) characterized by consisting of Lynn-ized boron system semi-conductors of the polycrystal with which the buffer coat prepared on the single crystal substrate includes the crystal face which sets indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is a positive integer).

(6) The above (1) characterized by consisting of ingredients with which a {110}-Lynn-ized boron system semiconducting crystal layer contains the Lynn-ized boron (boron monophosphide) of the monomer which makes the band gap in a room temperature 3.0**0.2 electron volts (eV) thru/or the laminating structure given in any 1 term of (5).

[0014] Moreover, this invention is the manufacture approach of the laminating structure given in (following 7) thru/or following (12) terms.

(7) The above (1) characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on a single crystal substrate thru/or the manufacture approach of the laminating structure given in any 1 term of (6).

(8) The manufacture approach of the laminating structure given in the above (7) characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on the single crystal substrate which makes a front face the {100} crystal faces.

(9) The manufacture approach of the laminating structure given in the above (7) characterized by forming a {110}-Lynn-ized boron system semiconducting crystal layer on this buffer coat in 750-degree-C or more

temperature requirement 1200 degrees C or less after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal on the single crystal substrate which makes a front face the {111} crystal faces.
(10) The above (7) characterized by forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at low temperature rather than a {110}-Lynn-ized boron system semiconducting crystal layer thru/or the manufacture approach of the laminating structure given in any 1 term of (9).
(11) The above (7) characterized by forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at 250-degree-C or more temperature of 700 degrees C or less thru/or the manufacture approach of the laminating structure given in any 1 term of (10).
(12) Heat-treat to a buffer coat at an elevated temperature more after forming the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal at 250 or more degrees-C temperature of 700 degrees C or less. The above (7) characterized by forming the buffer coat which consists of a Lynn-ized boron system semi-conductor of the polycrystal which has the crystal face which sets indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is a positive integer) thru/or the manufacture approach of the laminating structure given in any 1 term of (11).
[0015] Moreover, this invention is a light emitting device given in (following 13) thru/or following (17) terms.
(13) Light emitting device using the laminating structure the above (1) possessing the buffer coat which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or given in any 1 term of (6).
(14) Light emitting device using the laminating structure the above (1) possessing the barrier layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or given in any 1 term of (6).
(15) Light emitting device using the laminating structure the above (1) possessing the current inhibition (constriction) layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or given in any 1 term of (6).
(16) Light emitting device using the laminating structure the above (1) possessing the electrode contact layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or given in any 1 term of (6).
(17) The light emitting device using the laminating structure the above (1) possessing the semi-conductor multilayers reflecting mirror with which at least a part consists of a {110}-Lynn-ized boron system semiconducting crystal layer thru/or given in any 1 term of (6) [0016] Moreover, this invention is the lamp which used the light emitting device of a publication for (18) above (13) thru/or any 1 term of (17).
(19) The light source using a lamp given in the above (18). It comes out.
[0017]
[Embodiment of the Invention] The example which constitutes the laminating structure as 1st operation gestalt of this invention by using conductive n form or p form silicon as a substrate is given. In addition, it constitutes as a substrate using group-III-V-semiconducter single crystals, such as p form, n form gallium phosphide (GaP), gallium arsenide (GaAs), or Lynn-ized boron (BP) (refer to **J.Electrochem.Soc., 120 (1973), p.p.802-806., and ** U.S. Pat. No. 5,042,043 number official report). A conductive crystal ingredient is depended on the electric conductivity of a substrate, then a substrate, and positive/negative and which polar ohmic (Ohmic) electrode can be laid at the rear face. Therefore, a conductive crystal substrate removes a part of laminating structure at the time of using sapphire etc. as an insulating substrate, and gives a convenience technical means to constitute a light emitting device for the complicated process (to refer to JP,10-321907,A) of forming an electrode after exposing a conductive configuration layer front face, nothing and simple with needlessness. Especially the conductive single crystal substrate of low specific resistance that makes resistivity below 10 milli ohms (mohms) is effective in bringing about LED which stopped forward voltage (the so-called Vf) low.
[0018] Moreover, the greatest description in the 1st operation gestalt of this invention is to arrange the buffer coat which consists of an amorphous substance or a Lynn-ized boron system semi-conductor of polycrystal in the middle of a substrate and the 1 configuration layer slack {110}-Lynn-ized boron system semiconducting crystal layer of the laminating structure. A buffer coat can consist of Lynn-ized boron system semi-conductors written for example, by general formula BalphaaluminumbetaGagammaIn1-alpha-beta-gamma P1-deltaAsdelta (0< alpha<=1, 0<=beta<1, 0<=gamma<1, 0< alpha+beta+gamma <=1, 0<=delta<1). Moreover, it can constitute from a Lynn-ized boron system semi-conductor which contains the nitrogen (N) written by general formula BalphaaluminumbetaGagammaIn1-alpha-beta-gamma P1-deltaNdelta (0< alpha<=1, 0<=beta<1, 0<=gamma<1, 0< alpha+beta+gamma <=1, 0< delta<1), for example. Preferably, there are few configuration elements and it constitutes from a 2 yuan crystal which can be constituted simple, or 3 yuan mixed crystal. For example, it constitutes from monomer Lynn-ized boron (BP) aluminium phosphide and boron mixed crystal (BalphaaluminumbetaP: 0< alpha<=1, 0<= beta< 1 and alpha+beta= 1), Lynn-ized boron and gallium mixed crystal (BalphaGadeltaP: 0< alpha<=1, 0<= delta< 1 and alpha+delta= 1), or Lynn-ized boron, indium mixed crystal, etc. (BalphaIn1-alphaP:0<alpha<=1). The buffer coat which consists of an amorphous substance or polycrystal eases the stacking fault affinity of a substrate and a {110}-Lynn-ized boron system semiconducting crystal layer, and has the operation which brings about the {110}-Lynn-ized boron system semiconducting crystal layer crystal defect consistencies, such as a misfit (misfit) rearrangement, excel [layer] in crystallinity small.

[0019] The buffer coat of an amorphous substance or polycrystal can also consist of Lynn-ized boron system semi-conductors which carry out lattice matching to the single crystal ingredient which constitutes a substrate (refer to JP,2000-22211,A). For example, the buffer coat which achieves a GaP single crystal (lattice constant **5.450A) substrate and lattice matching can consist of Lynn-ized boron and a gallium (B0.32Ga0.68P: lattice constant **5.450A), **-ized boron, a gallium (B0.23Ga0.77As: lattice constant **5.450A), etc. (refer to above-mentioned JP,2000-22211,A). Moreover, there are B0.02Ga0.98P as an example of a component of the buffer coat which carries out lattice matching to a silicon (lattice constant **5.431A) substrate. In addition to the above-mentioned operation, the buffer coat which carries out lattice matching to a substrate has effectiveness especially in preventing exfoliation of the configuration layer of the laminating structure from a substrate. Moreover, the buffer coat which consists of a Lynn-ized boron system semi-conductor is faced preparing the Lynn-ized boron system semi-conductor layer as the upper layer, since it offers the "growth nucleus" to which equal growth is urged, is flat and can demonstrate the operation which brings about the continuous upper layer. Especially the buffer coat that consists of a Lynn-ized boron system semi-conductor when preparing the Lynn-ized boron system semi-conductor layer on the single crystal substrate which does not contain the configuration element, for example, a silicon substrate, achieves the duty of the adsorption site (site) of the element which constitutes the upper layer, and acts effective in promoting equal growth.

[0020] the buffer coat which consists of a Lynn-ized boron system semi-conductor -- MOCVD -- law (Inst.Phys.Conf.Ser. and No.129 (IOP Publishing Ltd., 1993) --) refer to the 157-162 page and a molecular beam -- epitaxial (MBE) -- law (J. -- Solid State Chem. and 133 (1997) --) refer to the 269-272 page and halide (halide) -- law (** "a Japanese crystal growth society magazine" --) Vol.24, No.2 (1997), 150 pages and **J.Appl.Phys., 42 (1) and (1971), refer to 420 - the 424 page, and a hydride (hydride) -- it depends on vapor growth means, such as law, and can form. Especially all the raw materials of a configuration element are gases, and if the flow rate or the rate of a feeder current quantitative ratio of the gas raw material is adjusted, since the crystal layer of a desired conduction type will be obtained simple (J. refer to Crystal Growth, 24/25 (1974), and 193-196 pages), a MOCVD means is convenience at formation of the Lynn-ized boron system semi-conductor layer. The organic phosphorous compound systems of reaction, such as boron triethyl (C2H5) (3B) / borane (BH3) or diboron hexahydride (B-2 H6) / phosphine (PH3), or a TASHA reeve chill (tert.-buthyl) phosphine, can be illustrated as a gaseous-phase-reaction system which can be used for the MOCVD method (refer to Jpn.J.Appl.Phys., 13 (3) and (1974), and 411 - 416 pages).

[0021] Especially the buffer coat that consists of an amorphous substance or polycrystal can be formed in the above-mentioned vapor growth means by making membrane formation temperature into 250 degrees C - 700 degrees C. The buffer coat which consists of a Lynn-ized boron system semi-conductor which makes an amorphous substance a subject becomes is easy to be obtained, so that it considers as low membrane formation temperature. Since disassembly of the raw material for membrane formation does not fully advance below 250 degrees C, membrane formation is unstable and inconvenient. At the membrane formation temperature exceeding about 450 degrees C, the buffer coat which consists of a Lynn-ized boron system semi-conductor which makes polycrystal a subject becomes being easy to conclude. It becomes and is [that the good crystal layer which cannot demonstrate the relaxation effect of grid mismatching sufficient at the temperature exceeding 700 degrees C is easy to be obtained] inconvenient. That a buffer coat is an amorphous layer or a polycrystal layer depends on a general X-ray diffraction method, a general electron diffraction method, etc., and it is analyzable. As for the thickness of a buffer coat, irrespective of the existence of the adjustment of a grid with a substrate ingredient, it is desirable about to set 100nm or less to 50nm or less by 2nm or more still more preferably by 1nm or more. The Lynn-ized boron system semi-conductor of suitable thickness is arranged as a buffer coat, and if the operation which eases a lattice strain is utilized, the crystal face which sets the indices of crystal plane of a front face parallel to the front face of a single crystal substrate to {110} on a buffer coat will be made to carry out the laminating of the Lynn-ized boron system semi-conductor layer of the single crystal which comes to carry out a laminating.

[0022] The indices of crystal plane which this invention says point out the mirror (Miller) characteristic which is an index for expressing the crystal face (C. W. van work, "chemical crystallography" (refer to June 15, Showa 45, Baifukan Issue First edition, and 21-22 pages).). For example, it is the generic name of the crystal face equivalent to the crystal face which sets indices of crystal plane to {110} to (110), such as (110), (-110), and (-1-10), (1-10). moreover -- for example, the crystal front face which sets indices of crystal plane to {111} -- or (111) (-1-1-1) -- etc. -- it is the thing of the front face which consists of the crystal faces equivalent to (111). If the buffer coat formed on the single crystal substrate of a cubic sphalerite mold is used, the Lynn-ized boron system semiconducting crystal layer which has fixed indices of crystal plane can be brought about irrespective of the indices of crystal plane of the crystal face which constitutes a single crystal substrate front face. For example, if it depends on a MOCVD means and the above-mentioned buffer coat concerning this invention for formation temperature is used as 1200 degrees C or less above 750 degrees C, the crystal face which sets the indices of crystal plane of a front face parallel to the front face of a single crystal substrate to {110} can form on it the Lynn-ized boron system semiconducting crystal layer ({110}-Lynn-ized boron system semiconducting crystal layer) which comes to carry out a laminating. A pattern that the {110} crystal faces of the Lynn-ized boron system semiconducting crystal layer have arranged in parallel with the crystal face which constitutes a substrate front face in drawing 4 is shown typically. That is, the

buffer coat which consists of a Lynn-ized boron system semi-conductor which consists of the amorphous substance or polycrystal concerning this invention has the operation which brings about the Lynn-ized boron system semiconducting crystal layer which indices of crystal plane become from the laminating of the fixed crystal face, using as small and weak effect of the crystal field of a single crystal are uninfluential of a substrate. Moreover, it combines and the buffer coat concerning this invention has the operation which is not in the former and widens the temperature requirement concluded in the good Lynn-ized boron system semiconducting crystal layer to the large range of 450 degrees C. Since the Lynn-ized boron system semiconducting crystal layer of a smooth front face is stabilized since the hole (pit) based on the vaporization of Lynn (P) which constitutes the Lynn-ized boron system semi-conductor from an elevated temperature exceeding 1200 degrees C is generated notably, and it does not conclude, it is unsuitable.

[0023] The laminating of the {110}-Lynn-ized boron system semiconducting crystal layer is carried out on the cubic substrate which sets the indices of crystal plane of the surface crystal face to {100}, for example, the {100}-single crystal substrate of a sphalerite mold, and the laminating structure consists of the 2nd operation gestalt of this invention. If the laminating of the {110}-Lynn-ized boron system semiconducting crystal layer is carried out in parallel with the front face of a {100}-single crystal substrate, generally it will combine with the diffraction resulting from a {100}-single crystal substrate at an X-ray diffraction pattern (pattern), and the diffraction from a {110}-Lynn-ized boron system semiconducting crystal layer will appear. From this, it is found whether the interrelation about the crystal face of the single crystal substrate and the Lynn-ized boron system semiconducting crystal layer concerning this invention is attained. The X-ray diffraction pattern (pattern) about the Lynn-ized boron crystal layer of the monomer formed in drawing 5 at 800 degrees C as an example through the Lynn-ized boron buffer coat formed at 350 degrees C on the {100}-Si single crystal substrate is hung up. In addition to the Bragg (Bragg) diffraction peak (whenever [angle-of-diffraction] 2 theta**69.1 degrees) from the {400}-Si crystal face originating in a {100}-Si single crystal substrate, the {220} diffraction peak (whenever [angle-of-diffraction] 2 theta**57.6 degrees) from BP crystal layer has appeared. This shows that the laminating of the {110}-Lynn-ized boron system semi-conductor layer is carried out in parallel with the front face of a {100}-single crystal substrate. From the laminating structure of such a configuration, there is an advantage which can constitute the laser diode of the shape of a rectangular parallelepiped which makes a cleavage plane a resonance end face simple.

[0024] For example, the pulse duty factor of the configuration atom in the {111} crystal-face front face of a sphalerite mold is size from the {100} crystal faces. For this reason, diffusion Lynn (P) which constitutes the buffer coat which consists of a Lynn-ized boron system semi-conductor from a {111}-single crystal substrate, or inside [of boron (B)] a substrate, and osmosis are controlled, and effect is taken to hang down even if the buffer coat by which thickness was controlled is stabilized. Therefore, it supposes that the laminating of the {110}-Lynn-ized boron system semi-conductor layer is carried out on the cubic substrate which sets indices of crystal plane to {111}, for example, the {111}-single crystal substrate of a sphalerite mold, and the laminating structure consists of the 3rd operation gestalt of this invention. The X-ray diffraction pattern (pattern) about the Lynn-ized boron crystal layer of the monomer formed in drawing 6 at 900 degrees C as an example through the Lynn-ized boron buffer coat formed at 350 degrees C on the {111}-Si single crystal substrate is hung up. In addition to the {222} diffraction peak (whenever [angle-of-diffraction] 2 theta**58.8 degrees) originating in a {111}-Si single crystal substrate, the {220} diffraction peak (whenever [angle-of-diffraction] 2 theta**57.6 degrees) from BP crystal layer has appeared. This shows that the laminating of the {110}-Lynn-ized boron system semiconducting crystal layer is carried out in parallel with the front face of a {111}-single crystal substrate. Even if the orientation relation of such the crystal face depends on an electron diffraction method, it can be investigated.

[0025] The {110}-Lynn-ized boron system semiconducting crystal layer brought about without depending on whether it is the single crystal substrate which has which indices of crystal plane of {100} or {111} acts as a dominance substrate layer for carrying out the laminating of the luminous layer (referring to JP,55-3834,B) which is emitting short wave Nagamitsu from a convenient gallium nitride (GaN) system semi-conductor. the monomer Lynn-ized boron (boron monophosphide:BP) which is a cube zinc sulfide ore type (spharelite) (refer to FIRRIPUSU work, a "semi-conductor joint theory" (Yoshioka Shoten, July 25, 1985 issue, the 3rd **), and 14 - 15 pages) crystal -- cubic (cubic) gallium nitride (c-GaN: lattice constant =4.510A) and abbreviation -- it has the same lattice constant of 4.538A (refer to the above-mentioned "semiconductor device introduction" and 28 pages). furthermore, spacing of the {110} crystal faces of BP -- about 3.209A -- it is -- hexagonal (hexagonal) -- 3.180A which is the a-axis lattice constant of GaN (h-GaN), and abbreviation -- since it is equivalent, the adjustment of a grid with a GaN system semi-conductor is good. Therefore, on a {110}-Lynn-ized boron system semi-conductor layer, the advantage which can carry out the laminating of the GaN system luminous layer which is excellent in crystallinity with few crystal defects resulting from the mismatch of a grid is.

[0026] The description on the configuration in the 4th operation gestalt of this invention is to have constituted from a Lynn-ized boron system semi-conductor layer of polycrystal including the crystal face which carries out indices of crystal plane except {110} for the buffer coat constituted from the amorphous substance or polycrystal prepared on a single crystal substrate especially. For example, it constitutes from a polycrystal layer including the crystal faces, such as {111}, {311}, or {100}. It has the operation which depends on making the interior of a buffer coat generate the crystal face of such Miller indices, and eases the stacking fault

affinity of the single crystal and laminating structure configuration layer which constitute a substrate, and absorbs a stacking fault and a reverse phase grain boundary, and brings about a laminating structure configuration layer with few crystal defect consistencies. The content ratio of the {110} crystal faces inside a polycrystal buffer coat and the other above crystal faces is called for from an intensity ratio with a {110} diffraction peak acquirable [with a general X-ray diffraction method], for example. A desirable configuration is the case where, as for about 1/5 and a more desirable thing, the content of about 1/10, i.e., the {111} crystal faces, carries out the intensity ratio of a {111} diffraction peak to 1 / 5 - 1/10 of the {110} crystal faces as opposed to the reinforcement of a {110} diffraction peak. Furthermore, it is desirable that the ratios of the sum total of the reinforcement of the diffraction peak from the other crystal faces are about 1 / 5 - 1/10 to the X diffraction peak intensity resulting from the {110} crystal faces.
[0027] Moreover, the 5th operation gestalt of this invention constitutes from the Lynn-ized boron system semi-conductor layer of the polycrystal including amorphous or the crystal face of the limited indices of crystal plane which set indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is a positive integer) for the buffer coat constituted from polycrystal prepared on a single crystal substrate. The crystal faces which set indices of crystal plane to 1/H, and {1 / K1/L} (each of H, K, and L is an integer) are the crystal faces, such as {111}, {-1-1-1}, {311}, and {-311}. These limited crystal faces can contribute for bringing about the laminating structure configuration layer which demonstrates the operation which absorbs plane defects, such as a stacking fault, etc. especially, and is excellent in crystallinity while easing the lattice strain of the single crystal and laminating structure configuration layer which constitute a substrate. Therefore about the buffer coat of the thin layer concerning this invention, the crystalline form inside a layer, an organization, and the configuration of the crystal face can be grasped to electron diffraction technique etc. at the cross-section TEM technique list which uses a transmission electron microscope (TEM), for example.
[0028] At 250-degree-C or more temperature of 700 degrees C or less, on a single crystal substrate, after forming a layer, the buffer coat which consists of a Lynn-ized boron system semi-conductor including the limited crystal face concerning the 5th above-mentioned operation gestalt can once be formed, if it heat-treats at an elevated temperature rather than formation temperature. For example, amorphous Lynn-ized boron and gallium (B0.5Ga0.5P) buffer coat which sets thickness to about 5nm are once formed at 400 degrees C on the front face of a gallium phosphide (GaP) single crystal substrate. Then, if a temperature up is carried out to 850 degrees C and it holds for 20 minutes for example, at this temperature, the buffer coat which consists of a Lynn-ized boron system semi-conductor including the crystal face where the above was limited can be constituted. The about 750 degrees C - 850 degrees C polycrystal buffer coat which includes the {110} crystal faces and the {111} crystal faces as a subject when it heat-treats at low temperature comparatively is obtained by the buffer coat. At about 1000-degree C elevated temperature, a polycrystal buffer coat including the {311} crystal faces becomes is easy to be formed in addition to the {111} crystal faces. Since the surface smoothness on the front face of a buffer coat based on the vaporization of Lynn (P) is degraded, it is not desirable to heat-treat a buffer coat at the elevated temperature exceeding 1200 degrees C. Moreover, if annealing (anneal) is given to a buffer coat at the elevated temperature exceeding 1200 degrees C, since the Lynn-ized boron polymer written by empirical formula B6P or B13P2 occurs (J. refer to Am.Ceramic Soc., 47 (1) and (1964), and 44 - 46 pages) and formation of a homogeneous buffer coat is checked, it is not desirable.
[0029] With the 6th operation gestalt of this invention, a {110}-Lynn-ized boron system semiconducting crystal layer is constituted from an ingredient containing the Lynn-ized boron (BP) which sets the band gap (band gap) in a room temperature to 3.0**0.2eV, and the laminating structure is formed using it. If BP of a monomer which has a high band gap is used, the Lynn-ized boron system semi-conductor layer which is not in the former and has a high band gap can be constituted. For example, in the conventional BP which sets a band gap to 2.0eV, it was as low as 2.3eV from which the highest is also equivalent to the band gap of GaP by 2.0eV or more, and was [that narrow Lynn-ized boron and gallium (BXGa1-XP:0 <=X<=1) mixed crystal of the range which can be taken are only brought about, and]. On the other hand, if it depends on this invention, the BXGa1-XP (0<=X<=1) mixed crystal of a high band gap covering a 3.0**0.2eV large area can be brought about by 2.3eV or more. The high Lynn-ized boron system semi-conductor layer of a band gap can be used as a window layer for luminescence transparency which acts conveniently for penetrating luminescence emitted from a single (Single Hetero:SH) or a duplex (Double Hetero:DH) assembling-die light-emitting part.
[0030] Especially the Lynn-ized boron (BP) that sets the band gap in a room temperature to 3.0**0.2eV or less can be formed by setting up within limits to which the growth rate in the case of a laminating and the both sides of the supply ratio of a raw material were prescribed (refer to application-for-patent No. 158282 [2001 to] specification). A growth rate is preferably made into 300A or less at 20A [or more]/m (refer to the above-mentioned application for patent No. 158282 [2001 to]). If a growth rate is made into the late rate of under 20A / min, desorption and volatilization are not fully inhibited for the (Lynn P) configuration element or its compound from a growth phase front face, and membrane formation may be unable to be achieved. If it is set as the quick growth rate exceeding 300A / min, the value of the band gap obtained becomes unstable and is not desirable. Moreover, when a growth rate is made quick to **, it is in the inclination which is easy to serve as a crystal layer of polycrystal, and it becomes inconvenient for obtaining a good crystal layer.
[0031] Moreover, it combines with a growth rate and the supply ratio of a raw material is preferably specified in 60 or less range or more by 15. Being, when forming BP layer, the supply ratio of a raw material is a ratio of

the amount of supply of the Lynn (P) raw material to the amount of supply of the boron (B) raw material to a growth reaction system. Moreover, if it is when forming BP system mixed crystal, it is the ratio of the amount of supply of the sum total of V group configuration element raw material containing boron (Lynn (P to the amount of supply of the sum total of the III group configuration element raw material containing B)). If the case where Lynn-ized boron and indium (BalphaIn1-alphaP:0<alpha<=1) mixed crystal are formed is made into an example, it will be the ratio of the amount of supply of the Lynn (P) raw material to the total amount of a gallium (Ga) raw material and an indium (In) raw material supplied to a growth reaction system. That is, it is the so-called V/III ratio. If a V/III ratio is made into less than 15 and smallness, a growth phase front face becomes disorderly and is not desirable. Moreover, if an III/V ratio is extremely made into size exceeding 60, it will see to stoichiometric and the growth phase whose Lynn (P) is in a rich condition will become is easy to be formed. It is supposed that the location which boron (B) should occupy is entered and superfluous Lynn (P) is worked as a donor (donor) by the crystal lattice (the Shono Katsufusa work, "semiconductor technology 100 collection of the VLSI age [5]" (refer to Ohm-Sha, Ltd., May 1, Showa 59 issue, the No. [5] (May, Showa 59 issue) volume [of electronic magazine electronics / 29th] appendix, and 121 pages).). If stoichiometric composition shifts to a rich Lynn (P) side, since trouble is caused to formation of p form crystal layer of low resistance, it is inconvenient.

[0032] The 13th of this invention thru/or the 17th operation gestalt constitute a light emitting device from the laminating structure which possesses a {110}-Lynn-ized boron system semiconducting crystal layer as various kinds of stratum functionale. For example, the {110}-Lynn-ized boron system semiconducting crystal layer concerning this invention formed through the buffer coat of an amorphous substance or polycrystal on the single crystal substrate turns into a crystal layer which is excellent in crystallinity. For this reason, in forming the light-emitting part which consists of SH or DH junction structure, it can use useful as a buffer coat as a substrate (deposition-ed) layer which can also hang down a good light-emitting part configuration layer. Therefore, the 13th operation gestalt can constitute a light emitting device from the laminating structure equipped with the light-emitting part which can be constituted from a good crystal layer by forming the {110}-Lynn-ized boron system semiconducting crystal layer concerning this invention as a buffer coat. For example, LED consists of the laminating structures equipped with the light-emitting part of the pn junction mold DH structure which makes a buffer coat the {110}-Lynn-ized boron system semiconducting crystal layer prepared through the Lynn-ized boron (BP) buffer coat of polycrystal on the {111}-silicon substrate, and makes a luminous layer for example, a phosphorus nitride-ized gallium (GaN1-XPX:0 <=X<=1) on it.

[0033] The 14th operation gestalt of this invention constitutes a light emitting device from the laminating structure equipped with the {110}-Lynn-ized boron system semiconducting crystal layer as a barrier layer. Especially, from the {110}-Lynn-ized boron semiconducting crystal layer of a high band gap, there is an advantage which can offer the barrier layer which fully makes the difference in an obstruction with a luminous layer size. For example, the clad (clad) layer of a high obstruction which sets the difference in a band gap to 0.3eV can consist of monomers BP (band gap **3.0eV, lattice constant **4.538A) to cubic GaN0.97P0.03 (band gap **2.7eV, lattice constant **4.538A) luminous layer. Moreover, if it uses as a cladding layer which makes the aperture which can penetrate luminescence for the high {110}-Lynn-ized boron system semiconducting crystal layer of a band gap to an external line of sight serve a double purpose, there is an advantage which can constitute LED of high brightness.

[0034] Since ionic bond nature is small and the conductive crystal layer of p form and n form is easy to be obtained, Lynn-ized boron (BP) can constitute pn junction structure simple. If this pn junction is established for example, on a light-emitting part, the light emitting device equipped with the {110}-Lynn-ized boron system semiconducting crystal layer concerning the 15th operation gestalt of this invention as a current blocking layer or a current constriction layer can be constituted. Furthermore, the pn junction which consists of a {110}-Lynn-ized boron system semiconducting crystal layer is arranged directly under the plinth (pad) electrode for circulating the LED operating current, and, specifically, is constituted. It arranges on the clad (clad) layer front face which hits the projection field of a plinth electrode and which makes a single hetero (SH) or a double hetero (DH) junction structure light-emitting part, for example. Thus, if it arranges, the circulation to the field [directly under] (projection field of the plinth electrode which cannot take out the so-called luminescence easily to the exterior) of the plinth electrode of the component operating current supplied through a plinth electrode will be prevented, and it will be conversely circulated preferentially to an open luminescence field. For this reason, it can contribute for constituting LED of high brightness.

[0035] Moreover, for example, since a laser diode (LD) is constituted as a current blocking layer, the {110}-Lynn-ized boron system semiconducting crystal layer which added and made oxygen (O) can be used. For example, on DH structure light-emitting part, once carrying out the laminating of the current blocking layer, it is deleted to band-like (the shape of a stripe), and the surface section of a light-emitting part is exposed. Then, the laminating of the conductive semi-conductor layer is carried out so that the saved current blocking layer and the front face of the exposed light-emitting part may be covered. Since such a configuration, then the operating current of high density can be concentrated and injected into the light-emitting part [directly under] of opening, LD of a current constriction mold can be constituted conveniently.

[0036] Suppose that a light emitting device is constituted from the laminating structure equipped with the {110}-Lynn-ized boron system semiconducting crystal layer as an electrode contact layer with the 16th operation gestalt of this invention. A Lynn-ized boron (BP) system crystal has ******** (Ikoma Toshiaki,

Ikoma intelligent collaboration, "a guide to basic physical properties of a compound semiconductor" (refer to September 10, 1991, Baifukan Issue First edition, and 14-17 pages)) of a valence band, and low ionic bond nature, therefore (refer to the above-mentioned "semi-conductor joint theory" and 49 - 51 pages) the advantage which can constitute the conductive layer of low resistance from a p form simply especially for a cubic sphalerite mold crystal. Therefore, it can contribute for forming the ohmic nature electrode of low contact resistance. For this reason, LED with low forward voltage (the so-called Vf) or LD with low threshold voltage (the so-called Vth) is brought about. p form ohmic electrode prepared on the contact layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer of p form can consist of for example, gold, a zinc (Au-Zn) alloy, etc. Moreover, on the contact layer which consists of a {110}-Lynn-ized boron system semiconducting crystal layer of n form, n form ohmic electrode can be formed from gold alloys, such as gold and a germanium (Au-germanium) alloy, gold and an indium (Au-In) alloy, or gold, a tin (Au-Sn) alloy, etc., etc.

[0037] Moreover, if the {110}-Lynn-ized boron system semiconducting crystal layer which was arranged in parallel with the front face of a single crystal substrate and which is excellent in surface surface smoothness is used, the reflecting mirror which can reflect luminescence in an external line of sight can be constituted with sufficient convenience ("surface emission-type laser" (refer to Ohm-Sha, Ltd., the 1st ** of the 1st edition of September 25, 1990 issue, and 105-117 pages).). Multistory [of the semi-conductor thin film of the different species which differ in a refractive index, or a different presentation] is carried out mutually periodically, and such a reflecting mirror constitutes it (refer to the above-mentioned "surface emission-type laser" and 118 - 119 pages). If this periodic multistory structure is constituted from a semi-conductor thin film which makes a difference of a refractive index size, the multilayers reflecting mirror which lessens periodicity (the number of multistory cycles) and makes a reflection factor high can be formed efficiently. in addition -- and if a multilayers reflecting mirror is constituted from a semi-conductor thin film which carries out lattice matching mutually, the semi-conductor multilayers reflecting mirror of high performance with a high reflection factor can be constituted. For example, a reflecting mirror can consist of structures to which it carried out multistory [of Lynn-ized boron (refractive-index **3.1) and the gallium nitride (refractive-index **2.5: refer to the above-mentioned "semiconductor device introduction" and 28 pages) which has the relation of abbreviation lattice matching] by turns. Therefore, from the laminating structure equipped with the {110}-Lynn-ized boron system semiconducting crystal layer as one configuration layer of a semi-conductor multilayers reflecting mirror, LED of high brightness which is excellent in the ejection effectiveness of luminescence to the exterior can be offered. With the 17th operation gestalt of this invention, it has the reflecting mirror which was greatly different and constituted the refractive index from mutual multistory structure of abbreviation lattice matching and the semi-conductor thin film which has the relation of lattice matching still more desirably and which covers a broadband and brings about a high reflection factor, and a light emitting device consists of the laminating structures possessing the semi-conductor multilayers reflecting mirror with which a part of configuration layer [at least] of this reflecting mirror consists of a {110}-Lynn-ized boron system semiconducting crystal layer.

[0038] The lamp of high brightness can consist of light emitting devices concerning the 13th of above-mentioned this invention thru/or the 17th operation gestalt. For example, the lamp of the 18th operation gestalt of this invention can have and constitute the following process. LED10 equipped with the current blocking layer 12 which consists of a {110}-Lynn-ized boron system semiconducting crystal layer concerning this invention on the substrate 11 is fixed to the center section of metal **** 16 which plated metals, such as silver on a plinth 15 (Ag), or aluminum (aluminum), with a conductive jointing material for corrugated fibreboard so that it may illustrate to drawing 7 . From this, the unipolar electrode 14 prepared in the base of a substrate 11 is electrically connected to the end child 17 attached to a plinth 15. Moreover, the electrode 13 installed on heterojunction structure is connected for one [attached to a plinth 15] of other terminals 18. A lamp can be constituted, if it closes so that **** 16 may be surrounded with the common epoxy resin 19 for the semi-conductor closures. Moreover, if it depends on this invention, a small light emitting diode lamp suitable as a drop which can also form small LED of about 200 micrometers - about 300 micrometer angle, therefore makes the installation volume smallness especially can be constituted.

[0039] Moreover, if an LED chip or the diode lamp by which the resin seal was carried out is gathered, the light source concerning this invention can be constituted. For example, two or more LED is electrically connected to juxtaposition, for example, the light source of a constant voltage drive mold can be constituted. Moreover, a diode lamp is electrically connected to a serial and the light source of a constant current mold can be constituted. Since it is not accompanied so much by heat dissipation by lighting unlike the source of a lamp light of the conventional incandescence mold, the light source using such LED can be especially used useful as a source of luminescence. For example, it can use as the light source for display of frozen foods. Moreover, the light source used suitable for a turn signal or lighting devices, such as a ringer for showing an outdoor drop and a traffic light and an automotive application, etc., for example can be constituted.

[0040]

[Function] In parallel with the crystal face on the front face of a substrate given in this invention, since the {110}-Lynn-ized boron system semiconducting crystal layer which comes to arrange the {110} crystal faces is in a light emitting device and can function as a buffer coat, it has the operation which brings about the light-emitting part which consists of a configuration layer which is excellent in crystallinity. Moreover, since it can

function as a barrier layer, it has the operation "shuts up" up the carrier which causes a radiative recombination. Moreover, since it can function as a current blocking layer, the operation which circulates a component drive current to the exterior with the priority to the luminescence field by which opening was carried out is demonstrated. Moreover, since it can function as an electrode contact layer, the operation which brings about the ohmic nature electrode of low contact resistance is demonstrated. Moreover, since it can function as a semi-conductor multilayers reflecting mirror, it has the operation which reflects luminescence in an external line of sight efficiently.

[0041] The buffer coat which consists of Lynn-ized boron system semi-conductors which become this invention from the amorphous substance or polycrystal of a publication has the operation which brings about the Lynn-ized boron system semiconducting crystal layer which has the {110} crystal faces parallel to the front face of a single crystal substrate which are excellent in crystallinity. Especially the buffer coat that consists of a Lynn-ized boron system semi-conductor which consists of polycrystal which comes to contain {1/H, 1 / K1/L} (for H, K, and L to be positive integer) crystal face in addition to the {110} crystal faces absorbs a lattice strain, a crystal defect, etc., and has the operation which brings about a good {110}-Lynn-ized boron system semiconducting crystal layer.

[0042] The Lynn-ized boron system semi-conductor layer which consists of ingredients which contain in this invention the Lynn-ized boron (BP) of the high band gap which sets a band gap to 3.0**0.2eV at the room temperature of a publication acts on dominance as a luminescence transparency (aperture) layer which has the high band gap which is not in the former.

[0043]

[Example] (Example 1) The case where light emitting diode (LED) is constituted from the laminating structure possessing the Lynn-ized boron (BP) system semi-conductor layer which becomes considering an amorphous substance as a subject in the state of an AZUGU loan (as-grown) is made into an example, and this invention is explained concretely. The cross section of LED1A concerning this example 1 is shown in drawing 1 .

[0044] Laminating structure 1B of the light emitting device application concerning this example 1 constituted the (Boron B) dope p form (111)-Si single crystal as a substrate 101. a substrate 101 top -- boron triethyl (C2H5) (3B) / phosphine (PH3) / hydrogen (H2) system ordinary pressure MOCVD -- the Lynn-ized boron buffer coat 102 which makes a subject the amorphous substance grown up at 350 degrees C by law was deposited. The thickness of a buffer coat 102 could be about 5nm.

[0045] The laminating of the p form lower cladding layer 103 which consists of {110}-Lynn-ized boron (BP) of the monomer which the front face arranged in parallel with the crystal face (111) of the front face of Si substrate at 850 degrees C becomes from the {110} crystal faces was carried out to the front face of a buffer coat 102 using the above-mentioned MOCVD vapor growth means. The impurity of p form was used as magnesium (Mg), and used screw-magnesium cyclopentadienyl (bis-(C5H4)2Mg) for the doping raw material. Carrier concentration of the lower cladding layer 103 was set to abbreviation 8x1018cm-3. Thickness could be 800nm. The buffer coat 102 which has the crystalline structure concerning this invention was written as the substrate layer, and the lower cladding layer 103 has consisted of Lynn-ized boron continuation layers without a crack (crack). Moreover, after ending formation of the lower cladding layer 103 at an elevated temperature rather than a buffer coat 102, the buffer coat 102 was changing to the polycrystal layer.

[0046] On the p form {110}-BP lower cladding layer 103, the laminating of the luminous layer 104 constituted from cubic n form GaN0.97P0.03 layer (lattice constant = 4.538A) which carries out lattice matching to Lynn-ized boron (BP; lattice constant =4.538A) was carried out. The crystal front face of 0.03 layers became what mainly consisted of the {110} crystal faces arranged in parallel with the GaNwhich makes luminous layer 1040.97P{110} of BP layer front face which makes lower cladding layer 103 crystal face. The carrier concentration of a luminous layer 104 was adjusted to abbreviation 1x1017cm-3 by adding silicon (Si) as a dopant of n form at the time of formation of a luminous layer 104. The thickness of a luminous layer 104 could be about 120nm.

[0047] On the front face of n form GaN0.97P0.03 luminous layer 104, the laminating of the up cladding layer 105 which consists of a BP layer of n form by the above-mentioned MOCVD system of reaction was carried out. The up cladding layer 105 consisted of Lynn-ized boron of a monomer which has the {110} crystal faces which come to carry out multistory [of the {110} crystal faces] perpendicularly to the front face of a luminous layer 104. The dopant of n form adjusted carrier concentration to abbreviation 8x1016cm-3 as silicon (Si). Thickness could be 80nm. The light-emitting part of pn junction mold double hetero (DH) structure was formed from the p form {110}-BP lower cladding layer 103 which formed 850 degrees C and growth temperature as the same, n form GaN0.97P0.03 luminous layer 104, and the n form {110}-BP up cladding layer 105.

[0048] The circular plinth electrode 106 has been arranged on the up cladding layer 105. The plinth electrode 108 consisted of gold and germanium (Au95 mass % and germanium5 mass %) vacuum deposition film. The diameter of the plinth electrode 106 was set to 120 micrometers. Moreover, all over the abbreviation for the rear face of the p form Si substrate 101, p form ohmic electrode 107 has been arranged and LED1A was constituted. p form ohmic electrode 107 consisted of (Aluminum aluminum) vacuum deposition film. Si single crystal substrate 101 was cut out in the direction parallel to the [211] directions, and perpendicular, and it was referred to as LED chip 1A of the square which sets one side to about 300 micrometers.

[0049] The emission center wavelength at the time of carrying out conduction of the operating current of

20mA (mA) between the plinth electrode 106 and p form ohmic electrode 107 in the forward direction was set to about 415nm. The brightness in the chip (chip) condition measured using a common integrating sphere became an about 8mm candela (mcd), and Lynn-ized boron system LED1A of high luminescence reinforcement was offered. the forward voltage (the so-called Vf) for which it asked from the I-V property — about 3.6 — it was set to V (forward current = 20mA). Moreover, reverse voltage is about 8V (reverse current =10microA), and LED of high pressure-proofing was offered.
[0050] (Example 2) Light emitting diode (LED) consisted of the laminating structures possessing the Lynn-ized boron (BP) system semi-conductor layer of the polycrystal which connotes the crystal face of specific indices of crystal plane. At this example 2, LED consisted of the laminating structures of the structure shown in the same drawing 1 as the above-mentioned example 1.
[0051] In this example 2, the 2 degree (100) OFF (off) Si single crystal of Lynn (P) dope n forms was used as a substrate. this substrate top — boron triethyl (C2H5) (3B) / trimethylgallium (CH3) (3Ga) / phosphine (PH3) / hydrogen (H2) system reduced pressure MOCVD — the Lynn-ized boron and the gallium mixed-crystal layer of n form were deposited in undoping which makes a subject polycrystal grown up at 550 degrees C by law. The pressure at the time of MOCVD growth was set as about 6x104 pascals (pressure unit-a). Thickness could be about 8nm. (Boron B) presentation ratio of Lynn-ized boron and gallium mixed crystal was set as 0.02 (B0.02Ga0.98P: lattice constant **5.431A) which carries out lattice matching to Si single crystal (lattice constant **5.431A) substrate.
[0052] After finishing deposition of Lynn-ized boron and a gallium (B0.02Ga0.98P) layer, the temperature up of this layer was carried out to 750 degrees C in the mixed ambient atmosphere (PH32.5 volume %+Ar97.5 volume %) of a phosphine (PH3) and an argon (Ar). It held for 15 minutes with the constant temperature of 750 degrees C. By this heat treatment, the B0.02Ga0.98P layer was made with the buffer coat of polycrystal including the {111} crystal faces and the {311} crystal faces.
[0053] Next, the temperature of a buffer coat was raised at 900 degrees C within the inert gas ambient atmosphere containing the above-mentioned phosphorus compounds. The laminating of the n form lower cladding layer which consists of Lynn-ized boron and a gallium (B0.98Ga0.02P) which the front face arranged in parallel with the crystal face (100) of the front face of Si substrate becomes from the {110} crystal faces with the above-mentioned MOCVD vapor growth means was carried out to the front face of a buffer coat. The n form {110}-B0.98Ga0.02P layer was formed under 900 degrees C and conditions with a pressure [at the time of growth] of about 8x104Pa. n form impurity was used as silicon (Si), made the disilane (Si2H6) the doping raw material at volume part per million, and used mixed gas with about 50 vol(s).ppm **** hydrogen (H2). Carrier concentration of a lower cladding layer was set to abbreviation 2x1018cm-3. Thickness could be 800nm. The buffer coat of polycrystal which has the crystalline structure concerning this invention was written as the substrate layer, and the lower cladding layer has consisted of continuation film of a Lynn-ized boron and a gallium without a crack (crack). Moreover, when depending on this example 2, the reinforcement of the X diffraction peak from the {220} crystal faces became about 1.2 times as high as the {110}-Lynn-ized boron layer which constitutes the lower cladding layer of an example 1. Moreover, since the band gap in an n form {110}-B0.98Ga0.02P layer room temperature set the growth rate to about 25nm per minute and formed the V/III ratio (=PH3/(CH3) (3Ga+(C2H5) 3B) supply ratio) as 45, it was set to about 3.0eV.
[0054] On the n form {110}-B0.98Ga0.02P lower cladding layer, the laminating of the luminous layer constituted from cubic n form GaN0.95P0.05 layer (lattice constant = 4.557A) which carries out lattice matching to B0.98Ga0.02P (lattice constant **4.557A) was carried out. It became what mainly consists of the {110} crystal faces arranged in parallel with the GaN0.95P{110} of B0.98Ga0.02 P layer front face where crystal front face of 0.05 layers also makes lower cladding layer crystal face of a luminous layer. At the time of formation of a luminous layer, silicon (Si) was added as a dopant of n form, and the carrier concentration of a luminous layer was adjusted to abbreviation 3x1017cm-3. Moreover, the thickness of a luminous layer could be about 100nm.
[0055] On the front face of n form GaN0.95P0.05 luminous layer, the laminating of the up cladding layer which consists of B0.98Ga0.02P layer of p form by the above-mentioned MOCVD system of reaction was carried out. The up cladding layer consisted of crystal layers which have the {110} crystal faces which come to carry out multistory [of the {110} crystal faces] perpendicularly to the front face of a luminous layer. The dopant of p form adjusted carrier concentration to abbreviation 4x1018cm-3 as magnesium (Mg). Thickness could be 200nm. Moreover, since the band gap in a p form {110}-B0.98Ga0.02P layer room temperature set the growth rate to about 25nm per minute and formed the V/III ratio (PH3/(CH3) (3Ga+(C2H5) 3B) supply ratio) as 45, it was set to about 3.0eV. For this reason, the B0.98Ga0.02P up cladding layer was used also as a luminescence transparency window layer for penetrating luminescence to an external line of sight. The light-emitting part of pn junction mold double hetero (DH) structure was formed from the n form {110}-B0.98Ga0.02P lower cladding layer which formed 900 degrees C and growth temperature as the same, n form GaN0.95P0.05 luminous layer, and the p form {110}-B0.98Ga0.02P up cladding layer.
[0056] The circular ohmic nature plinth electrode has been arranged on an up cladding layer. The plinth electrode consisted of gold and zinc (Au95 mass % and Zn5 mass %) vacuum deposition film. The diameter of a plinth electrode was set to 110 micrometers. Moreover, all over the abbreviation for the rear face of an n form Si substrate, n form ohmic electrode has been arranged and LED was constituted. n form ohmic electrode consisted of vacuum deposition film of (Aluminum aluminum) antimony (Sb) alloy. It made with the chip (chip)

of the square which carries out cleavage in parallel with the [110] crystal orientation of a {110}-B0.98Ga0.02P crystal layer which makes an up cladding layer, and sets one side to about 300 micrometers.
[0057] The emission center wavelength at the time of carrying out conduction of the operating current of 20mA (mA) between a plinth electrode and n form ohmic electrode in the forward direction was set to about 470nm. The brightness in the chip (chip) condition measured using a common integrating sphere became an about 8mm candela (mcd), and LED of high luminescence reinforcement was offered. the forward voltage (the so-called Vf) for which it asked from the I-V property -- about 3.5 -- it was set to V (forward current = 20mA). Moreover, reverse voltage is about 8V (reverse current =10microA), and LED of high pressure-proofing was offered.
[0058] (Example 3) LED consisted of the laminating structures possessing the semi-conductor multilayers reflecting mirror which uses as a configuration layer the Lynn-ized boron (BP) semi-conductor layer which has the {110} crystal faces, and the buffer coat which consists of a BP layer of the monomer which has the {110} crystal faces. The cross-section structure of LED3A of this example 3 is typically shown in drawing 2 . About the same component as LED1A given in an example 1, the same sign is attached by drawing 2 .
[0059] In this example 3, 2 degree (100) OFF (off) gallium phosphide (GaP) single crystal of sulfur (S) dope n forms was used as a substrate 101. a substrate 101 top -- boron triethyl (C2H5) (3B) / trimethylgallium (CH3) (3Ga) / phosphine (PH3) / hydrogen (H2) system reduced pressure MOCVD -- the Lynn-ized boron and the gallium (BXGa1-XP:0 <=X<=1) buffer coat 102 of n form were deposited in undoping which makes a subject polycrystal grown up at 450 degrees C by law. The pressure at the time of MOCVD growth was set as about 6x104 pascals (pressure unit-a). Thickness could be about 12nm. (Boron B) presentation ratio (=X) of Lynn-ized boron and gallium mixed crystal (BXGa1-XP) was set as 0.50 (B0.50Ga0.50P: lattice constant **4.994A) which has the middle lattice constant of the GaP single crystal (lattice constant **5.450A) of a substrate 101, and Monomer BP (lattice constant **4.538A).
[0060] On Lynn-ized boron and the gallium (B0.50Ga0.50P) polycrystal buffer coat 102, the laminating of the (Silicon Si) dope n form Lynn-ized boron (BP) buffer coat (carrier concentration **1x1018cm-3, thickness **950nm) 108 which a front face becomes from the {110} crystal faces was carried out. The {110}-monomer BP buffer coat 108 was formed at 850 degrees C with the above-mentioned reduced pressure MOCVD means.

[0061] On the single crystal buffer coat 108, the semi-conductor multilayers reflecting mirror 109 constituted from BP thin film 109a and Si dope n form gallium nitride (GaN) single crystal thin film 109b was formed. Each thickness of BP thin film 109a which constitutes a reflecting mirror 109, and GaN thin film 109b could be about 52nm. Moreover, carrier concentration set any thin films 109a and 109b to abbreviation 1x1018cm-3. The reflecting mirror 109 constituted the unit laminated structure which joined GaN thin film 109b and {110}-BP thin film 109a on the front face of the {110}-BP buffer coat 103 from a laminated structure which carried out multistory to five periods.
[0062] On {110}-BP thin film 109a which makes the surface of the semi-conductor multilayers reflecting mirror 109, it depended on the above-mentioned MOCVD means, and the laminating of the obstruction (lower clad) layer 103 which consists of a {110}-BP crystal layer of a monomer at 850 degrees C was carried out. Especially the lower cladding layer 103 set the growth rate to 10nm/m, and set up and formed the V/III (=PH3/(CH3)3Ga) ratio in 35, and constituted it from a {110}-BP crystal layer of the monomer which sets the band gap of a room temperature to about 3.1eV. Carrier concentration of the Si dope n form lower cladding layer 103 was set to abbreviation 2x1018cm-3, and thickness could be about 400nm.
[0063] On the n form {110}-BP lower cladding layer 103, the laminating of the luminous layer 104 constituted from a cubic n form Ga0.94In0.06N layer (lattice constant **4.538A) which carries out lattice matching to Monomer BP (lattice constant **4.538A) was carried out. The Ga0.94In0.06N layer [of a luminous layer 104] crystal front face also became what mainly consists of the {110} crystal faces arranged in parallel with the {110} crystal faces of the {110}-BP layer front face which makes a lower cladding layer. At the time of formation of a luminous layer 104, Si was added as a dopant of n form and carrier concentration was adjusted about 3x1017cm-3. Moreover, the thickness of a luminous layer 104 could be about 100nm.
[0064] On the front face of the n form Ga0.94In0.06N luminous layer 104, it depended on the above-mentioned MOCVD system of reaction, and the laminating of the up cladding layer 105 which consists of a monomer BP layer of p form at 850 degrees C was carried out. The up cladding layer 105 consisted of {110}-crystal layers which come to carry out multistory [of the {110} crystal faces] perpendicularly to the front face of a luminous layer. The dopant of p form adjusted carrier concentration to abbreviation 3x1018cm-3 as magnesium (Mg). Thickness could be 300nm. Moreover, since the band gap in the room temperature of a p form {110}-BP layer set the growth rate to about 40nm per minute and the V/III ratio (=PH3/(CH3) (3Ga+(C2H5) 3B) supply ratio) was formed as 45, the band gap in a room temperature was set to about 3.1eV. For this reason, the {110}-BP up cladding layer 105 has been used also as a luminescence transparency window layer for penetrating luminescence to an external line of sight. The light-emitting part of pn junction mold double hetero (DH) structure was formed from the n form {110}-BP lower cladding layer 103 which formed 850 degrees C and growth temperature as the same, the n form Ga0.94In0.06N luminous layer 104, and the p form {110}-BP up cladding layer 105.
[0065] The circular ohmic nature plinth electrode has been arranged on the {110}-BP up cladding layer 105. The plinth electrode consisted of gold and zinc (Au95 mass % and Zn5 mass %) vacuum deposition film. The

diameter of a plinth electrode was set to 130 micrometers. Moreover, all over the abbreviation for the rear face of an n form GaP substrate, n form ohmic electrode has been arranged and LED3A was constituted. n form ohmic electrode consisted of vacuum deposition film of golden (Au) and a germanium (germanium) alloy. It made with the chip (chip) of the square which carries out cleavage in parallel with the [110] crystal orientation of a {110}-BP crystal which makes the up cladding layer 105, and sets one side to about 350 micrometers.
[0066] The emission center wavelength at the time of carrying out conduction of the operating current of 20mA (mA) between a plinth electrode and n mold ohmic electrode in the forward direction was set to about 470nm. The brightness in the chip (chip) condition measured using a common integrating sphere became an about 8mm candela (mcd), and LED of high luminescence reinforcement was offered. the forward voltage (the so-called Vf) for which it asked from the I-V property -- about 3.5 -- it was set to V (forward current = 20mA). Moreover, reverse voltage is about 8V (reverse current =10microA), and LED of high pressure-proofing was offered.
[0067] (Example 4) The laminating structure of a laser diode (LD) application provided as an electrode contact layer by using as a current constriction layer the Lynn-ized boron (BP) system semi-conductor layer which consists of the {110} crystal faces was constituted. The cross-section structure of laminating structure 4B of this example 4 is typically shown in drawing 3 . About the same component as LED 1A and 3A given in the 1st or an example 3, the same sign is attached by drawing 3 .
[0068] Laminating structure 4B constituted 2 degree (100) OFF (off) silicon (Si) single crystal of antimony (Sb) dope n forms as a substrate 101. a substrate 101 top -- boron triethyl (C2H5) (3B) / trimethylgallium (CH3) (3Ga) / phosphine (PH3) / hydrogen (H2) system ordinary pressure (abbreviation atmospheric pressure) MOCVD -- the Lynn-ized boron and the gallium (BXGa1-XP:0 <=X<=1) buffer coat 102 of n form were deposited in undoping which makes a subject the amorphous substance grown up at 350 degrees C by law. Thickness could be about 15nm. (Boron B) presentation ratio (=X) of Lynn-ized boron and gallium mixed crystal (BXGa1-XP) was set as 0.02 (B0.02Ga0.98P: lattice constant **5.431A) which carries out lattice matching to Si single crystal (lattice constant **5.431A) of a substrate 101.
[0069] After finishing deposition of the amorphous Lynn-ized boron and gallium (B0.02Ga0.98P) buffer coat 102, the temperature up of the buffer coat 102 was carried out to 850 degrees C in the mixed ambient atmosphere (PH33.0 volume %+Ar97.0 volume %) of a phosphine (PH3) and nitrogen (N2). With the constant temperature of 850 degrees C, for 20 minutes, it held and the amorphous B0.02Ga0.98P layer was made with the buffer coat 102 of polycrystal including the {111} crystal faces and the {311} crystal faces.
[0070] On Lynn-ized boron and the gallium (B0.02Ga0.98P) polycrystal buffer coat 102, the laminating of the (Silicon Si) dope n form Lynn-ized boron (BP) crystal buffer coat (carrier concentration **1x1018cm-3, thickness **650nm) 108 which has the {110} crystal faces was carried out. The {110}-monomer BP buffer coat 108 was formed at 850 degrees C with the above-mentioned ordinary pressure MOCVD means.
[0071] On the buffer coat 108, it depended on the above-mentioned MOCVD means, and the laminating of the obstruction (lower clad) layer 103 which consists of a {110}-BP crystal layer of a monomer at 850 degrees C was carried out. Especially the lower cladding layer 103 set the growth rate to 25nm/m, and set up and formed the V/III (PH3/(CH3)3Ga) ratio in 50, and constituted it from a {110}-BP crystal layer of the monomer which sets the band gap of a room temperature to about 3.1eV. Carrier concentration of the Si dope n form lower cladding layer 103 was set to abbreviation 2x1018cm-3, and thickness could be about 500nm.
[0072] On the n form {110}-BP lower cladding layer 103, the laminating of the luminous layer 104 constituted from cubic n form GaN0.97P0.03 layer (lattice constant **4.538A) which carries out lattice matching to Monomer BP (lattice constant **4.538A) was carried out. It became what mainly consists of the {110} crystal faces arranged in parallel with the GaN0.97P{110} of {110}-BP layer front face where crystal front face of 0.03 layers also makes lower cladding layer crystal face of a luminous layer 104. At the time of formation of a luminous layer 104, Si was added as a dopant of n form, and carrier concentration was adjusted to abbreviation 1x1017cm-3. Moreover, the thickness of a luminous layer 104 could be about 95nm.
[0073] On the front face of n form GaN0.97P0.03 luminous layer 104, it depended on the above-mentioned MOCVD system of reaction, and the laminating of the up cladding layer 105 which consists of a monomer BP layer of p form at 850 degrees C was carried out. The up cladding layer 105 consisted of crystal layers which have the {110} crystal faces which come to carry out multistory [of the {110} crystal faces] perpendicularly to the front face of a luminous layer. The dopant of p form adjusted carrier concentration to abbreviation 2x1018cm-3 as magnesium (Mg). Thickness could be 300nm. Moreover, since the band gap in the room temperature of a p form {110}-BP layer set the growth rate to about 25nm per minute and the V/III (=PH3/(CH3) (3Ga+(C2H5) 3B)) ratio was formed as 50, the band gap in a room temperature was set to about 3.1eV. The light-emitting part of pn junction mold double hetero (DH) structure was formed from the n form {110}-BP lower cladding layer 103 which formed 850 degrees C and growth temperature as the same, n form GaN0.97P0.03 luminous layer 104, and the p form {110}-BP up cladding layer 105.
[0074] On the {110}-BP up cladding layer 105, it depends on the above-mentioned MOCVD means, and it carried out the laminating, having used as the current constriction layer 110 the {110}-BP crystal layer of high resistance which doped oxygen (O) at 850 degrees C. At the time of membrane formation, the oxygenation {110}-BP crystal layer made oxygen (O2) volume part per million, and produced it using mixed gas with an about 10 vol(s).ppm **** argon (Ar). a secondary ion mass spectrometry (SIMS) with the common oxygen atom concentration of the current constriction layer 110 interior -- about -- the quantum was carried out to

3x1018 atom / cm3. Moreover, the current constriction layer 110 constituted resistivity (specific resistance) from a {110}-BP crystal layer made into about 102 ohm centimeters (ohm-cm). Thickness could be about 500nm.
[0075] After forming the current constriction layer 110, it limited to the specific field and the current constriction layer 110 was removed by argon (Ar) / methane (CH4) / the hydrogen (H2) system plasma-etching method. The field which removed the current constriction layer 110 was limited to the strip region 111 of the lower part of a schedule field which prepares the band electrode (not shown) for constituting the laser diode (LD) of a common stripe (band-like) structured type (refer to "a semiconductor laser foundation, application -" (October 30, 1997, the 6th ** of Baifukan Issue First edition), and 10 - 11 pages). The strip region 111 which removed the current constriction layer 110 was made to expose the front face of the up cladding layer 105 which consists of a {110}-BP crystal layer.
[0076] The front face of the current constriction layer 110 which countered in the middle and it was made to save across the strip region 111 to which the front face of the up cladding layer 105 was exposed, and a strip region 111 was covered with the **-ized Lynn-ized boron (BAs0.05P0.95) mixed-crystal layer of p form. a {110}-BAs0.05P 0.95 mixed-crystal layer -- 3(C2H5) B / arsine (AsH3) / hydrogen (H2) system ordinary pressure (abbreviation atmospheric pressure) MOCVD -- it was made to grow up at 850 degrees C by law the carrier concentration of the BAs0.05P 0.95 mixed-crystal layer used as an electrode contact layer 112 for forming an ohmic nature surface electrode (not shown) -- about 2 -- it was referred to as x1018cm-3 and thickness could be about 150nm. The above constituted laminating structure 4B of a laser diode (LD) application.
[0077]
[Effect of the Invention] If it depends on this invention, since the laminating structure is constituted using the Lynn-ized boron system semiconducting crystal layer which can be formed in the large temperature requirement which is not in the former through the buffer coat which consists of a Lynn-ized boron system semi-conductor layer of an amorphous substance or polycrystal and which has the fixed indices of crystal plane of {110} which can give clear cleavage, without being dependent on the indices of crystal plane on the front face of a substrate, the suitable laminating structure for cleavage to constitute a component simple can be offered.
[0078] The laminating structure equipped with the Lynn-ized boron system semiconducting crystal layer which has the fixed indices of crystal plane of {110} which can give clear cleavage, without being dependent on the indices of crystal plane on the front face of a substrate which can be formed in the large temperature requirement which is not in the former can be efficiently obtained by minding the buffer coat which consists of a Lynn-ized boron system semi-conductor of the polycrystal which connotes the specific crystal face especially, if it depends on this invention.
[0079] Since a light emitting device is constituted from the laminating structure equipped with the Lynn-ized boron system semiconducting crystal layer which has the fixed indices of crystal plane of {110} which can give clear cleavage, without being dependent on the indices of crystal plane on the front face of a substrate which can be formed in the large temperature requirement which is not in the former by minding the buffer coat which consists of a Lynn-ized boron system semi-conductor layer of an amorphous substance or polycrystal if it depends on this invention, the light emitting device of high brightness can be offered.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section of LED given in an example 1.
[Drawing 2] It is the cross section of LED given in an example 3.
[Drawing 3] It is the cross section of the laminating structure of LD application given in an example 4.
[Drawing 4] It is the cross section of a crystal layer showing the relation of an array to the {111} crystal faces and the single crystal substrate front face which constitute the Lynn-ized boron system crystal layer concerning this invention.
[Drawing 5] It is the example of an X diffraction spectrum of the {110}-Lynn-ized boron system semiconducting crystal layer on a {100}-Si single crystal substrate.
[Drawing 6] It is the example of an X diffraction spectrum of the {110}-Lynn-ized boron system semiconducting crystal layer on a {111}-Si single crystal substrate.
[Drawing 7] It is the mimetic diagram which illustrates the cross-section structure of the lamp concerning this invention.
[Description of Notations]
1A, 3A, 4A, 10 Light emitting device (LED)
4B (Laser diode LD) application laminating structure
11 Substrate
12 Lynn-ized Boron Semi-conductor Current Blocking Layer
13 Surface Lateral Electrode
14 Substrate Rear-Face Electrode
15 Plinth
16 ****
17 18 Terminal
19 Closure Resin
101 Single Crystal Substrate
102 Amorphous Substance or Polycrystal Buffer Coat
103 Lower Cladding Layer
104 Luminous Layer
105 Up Cladding Layer
106 Surface Electrode
107 Rear-Face Electrode
108 Lynn-ized Boron System Semi-conductor Buffer Coat
109 Semi-conductor Multilayers Reflecting Mirror
109a The GaN thin film which constitutes a reflecting mirror
109b The {110}-BP thin film which constitutes a reflecting mirror
110 Current Constriction Layer
111 Strip Region
112 Electrode Contact Layer

[Translation done.]

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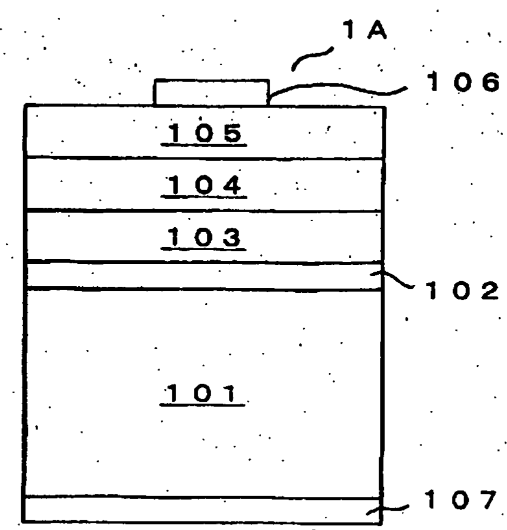
(54)【発明の名称】　積層構造体とその製造方法並びに発光素子、ランプ及び光源

(57)【要約】
【課題】従来に無く広い温度範囲で良質の結晶層を得ることを可能と成した上で、基板表面の面指数に依存せずに一定の面指数の結晶面からなり、その面指数が明瞭な劈開を呈する方向に合致する様に形成されたリン化硼素系半導体層から積層構造体を構成する。
【解決手段】単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、{１１０}－リン化硼素系半導体結晶層を形成する。



【特許請求の範囲】

【請求項１】単結晶基板と、該単結晶基板の表面に設けられた非晶質または多結晶のリン化硼素系半導体からなる緩衝層と、該緩衝層上に設けられた、単結晶基板の表面に平行な表面の面指数を｛１１０｝とする結晶面が積層されてなるリン化硼素系半導体結晶層（｛１１０｝－リン化硼素系半導体結晶層という。）とを具備することを特徴とする積層構造体。

【請求項２】｛１１０｝－リン化硼素系半導体結晶層が、面指数を｛１００｝とする立方晶の単結晶基板の表面上に設けられていることを特徴とする請求項１に記載の積層構造体。

【請求項３】｛１１０｝－リン化硼素系半導体結晶層が、面指数を｛１１１｝とする立方晶の単結晶基板の表面上に設けられていることを特徴とする請求項１に記載の積層構造体。

【請求項４】単結晶基板上に設けた緩衝層が、面指数を｛１１０｝以外とする結晶面を含む多結晶のリン化硼素系半導体から構成されていることを特徴とする請求項１乃至３の何れか１項に記載の積層構造体。

【請求項５】単結晶基板上に設けた緩衝層が、面指数を｛1／H，１／K，１／L｝（H，K，及びLは何れも正の整数）とする結晶面を含む多結晶のリン化硼素系半導体から構成されていることを特徴とする請求項４に記載の積層構造体。

【請求項６】｛１１０｝－リン化硼素系半導体結晶層が、室温での禁止帯幅を３．０±０．２エレクトロンボルト（ｅＶ）とする単量体のリン化硼素（ｂｏｒｏｎ ｍｏｎｏｐｈｏｓｐｈｉｄｅ）を含む材料から構成されていることを特徴とする請求項１乃至５の何れか１項に記載の積層構造体。

【請求項７】単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする請求項１乃至６の何れか１項に記載の積層構造体の製造方法。

【請求項８】表面を｛１００｝結晶面とする単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする請求項７に記載の積層構造体の製造方法。

【請求項９】表面を｛１１１｝結晶面とする単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする請求項７に記載の積層構造体の製造方法。

【請求項１０】非晶質または多結晶のリン化硼素系半導体からなる緩衝層を、｛１１０｝－リン化硼素系半導体結晶層よりも低温で形成することを特徴とする請求項７乃至９の何れか１項に記載の積層構造体の製造方法。

【請求項１１】非晶質または多結晶のリン化硼素系半導体からなる緩衝層を、２５０℃以上７００℃以下の温度で形成することを特徴とする請求項７乃至１０の何れか１項に記載の積層構造体の製造方法。

【請求項１２】２５０℃以上７００℃以下の温度で非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、より高温で緩衝層に熱処理を施して、面指数を｛1／H，１／K，１／L｝（H，K，及びLは何れも正の整数）とする結晶面を有する多結晶のリン化硼素系半導体からなる緩衝層を形成することを特徴とする請求項７乃至１１の何れか１項に記載の積層構造体の製造方法。

【請求項１３】｛１１０｝－リン化硼素系半導体結晶層からなる緩衝層を具備する請求項１乃至６の何れか１項に記載の積層構造体を用いた発光素子。

【請求項１４】｛１１０｝－リン化硼素系半導体結晶層からなる障壁層を具備する請求項１乃至６の何れか１項に記載の積層構造体を用いた発光素子。

【請求項１５】｛１１０｝－リン化硼素系半導体結晶層からなる電流阻止（狭窄）層を具備する請求項１乃至６の何れか１項に記載の積層構造体を用いた発光素子。

【請求項１６】｛１１０｝－リン化硼素系半導体結晶層からなる電極コンタクト層を具備する請求項１乃至６の何れか１項に記載の積層構造体を用いた発光素子。

【請求項１７】少なくとも一部が｛１１０｝－リン化硼素系半導体結晶層からなる半導体多層膜反射鏡を具備する請求項１乃至６の何れか１項に記載の積層構造体を用いた発光素子。

【請求項１８】請求項１３乃至１７の何れか１項に記載の発光素子を用いたランプ。

【請求項１９】請求項１８に記載のランプを用いた光源。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、単結晶基板表面の面指数とは相違する面指数の表面を有するリン化硼素（ＢＰ）系半導体結晶層を備えた積層構造体およびその製造方法に関する。また、その積層構造体から作製した発光素子、ランプまたは光源に関する。

【０００２】

【従来の技術】リン化硼素（ＢＰ）は、イオン結合度が０．００６と低く（フィリップス著、「半導体結合論」（（株）吉岡書店、１９８５年7月２５日発行、第３刷）、４９～５１頁参照）、特に、ｐ形伝導性の半導体層を得られ易い特徴を有している。この様なリン化硼素（ＢＰ）の特性は、例えば、ｐｎ接合型の発光部を簡便に構成するに優位に作用する。このため、従来から、リ

ン化硼素系ＩＩＩ－Ｖ族化合物半導体層を備えた積層構造体から発光ダイオード（ＬＥＤ）或いはレーザダイオード（ＬＤ）等の発光素子を構成する技術が開示されている（特開平２－２８８３８８号公報参照）。従来において、発光素子用途の積層構造体は、例えば、リン化ガリウム（ＧａＰ）及び窒化ガリウム（ＧａＮ）等のＩＩＩ－Ｖ族化合物半導体単結晶を基板として構成されている（①特開平２－２７５６８２号、②特開平１０－２４７７４５号各公報参照）。また、別の基板材料として珪素（Ｓｉ）単結晶（シリコン）が知られている（米国特許６，０６９，０２１号参照）。また、炭化珪素（ＳｉＣ）も基板材料として用いられている（特許第２，８０９，６９０号参照）。

【０００３】従来において、リン化硼素系半導体層は様々な機能層として利用されている。例えば、特開平１０－２４２５６９号公報に記載の発明には、リン化硼素（ＢＰ）層を電流阻止層として備えた電流狭窄型の緑色レーザダイオード（ＬＤ）が開示されている。また、リン化硼素（ＢＰ）層をオーミック（Ｏｈｍｉｃ）電極を形成するためのコンタクト（ｃｏｎｔａｃｔ）層として積層構造体に具備させる公知例もある（特開平１０－２４２５６８号公報参照）。また、リン化硼素（ＢＰ）層を緩衝層として備えた発光ダイオード（ＬＥＤ）も公知となっている（特開平１０－２４２５１４号公報参照）。特に、基板材料と積層構造体構成層との格子ミスマッチ（ｍｉｓｍａｔｃｈ）をより良く緩和するために、比較的に低温で形成した、所謂、低温緩衝層をリン化硼素（ＢＰ）系半導体層から構成する例が知られている（上記の米国特許６，０６９，０２１号参照）。例えば、シリコンやリン化ガリウム（ＧａＰ）単結晶基板上に、リン化ガリウム・硼素（$B_XGa_{1-X}P$：$0 \leq X \leq 1$）から緩衝層を構成する技術が開示されている（特開平１１－２６６００６号公報参照）。

【０００４】一方で、シリコンを基板とした場合、単結晶のリン化硼素（ＢＰ）層が帰結される温度は、１０２０℃～１０７０℃と高々、５０℃の極めて狭い範囲に限定されている（西永　頌、「応用物理」、第４５巻第９号（１９７６）、８９１～８９７頁参照）。この狭い温度範囲においてのみ、リン化硼素（ＢＰ）単結晶層が得られるとされ、それ以外の低温或いは高温で得られるリン化硼素層は多結晶層であるとされている（上記の「応用物理」、第４５巻参照）。また、（１００）－リン化ガリウム（ＧａＰ）単結晶を基板とし、ジボラン（B_2H_6）／ホスフィン（PH_3）／水素（H_2）反応系有機金属熱分解気相成長（ＭＯＣＶＤ）法に依り、１１５０℃でリン化硼素（ＢＰ）層を形成した従来例もある（Ｉｎｓｔ．Ｐｈｙｓ．Ｃｏｎｆ．Ｓｅｒ．，Ｎｏ．１２９（ＩＯＰ Ｐｕｂｌｉｓｈｉｎｇ Ｌｔｄ．，１９９３）、Ｃｈａｐｔｅｒ ３、１５７～１６２頁参照）。この場合でも、得られるリン化硼素（ＢＰ）層は、（１００）結晶面とそれ以外の結晶面とが混在する、所謂、多結晶層である（上記のＩｎｓｔ．Ｐｈｙｓ．Ｃｏｎｆ．Ｓｅｒ．Ｎｏ．１２９参照）。

【０００５】立方晶の単結晶を基板とした場合、極めて狭い温度範囲でのみ形成されるリン化硼素（ＢＰ）単結晶層の面指数は成長手段に依存せず、基板表面の面指数と同一であるとされている。例えば、ハロゲン（ｈａｌｏｇｅｎ）気相成長法では、面指数を（１１１）とするシリコン基板上には、同じく面指数を（１１１）とするリン化硼素（ＢＰ）単結晶層が形成される（Ｊ．Ｃｒｙｓｔａｌ Ｇｒｏｗｔｈ．１３／１４（１９７２）、３４６頁参照）。また、ＭＯＣＶＤ法でも、面指数を（１００）或いは（１１０）とするシリコン基板の表面上には、やはり同一の面指数の単量体のリン化硼素（ｂｏｒｏｎ ｍｏｎｏｐｈｏｓｐｈｉｄｅ）が形成されるとされる（Ｊｐｎ．Ｊ．Ａｐｐｌ．Ｐｈｙｓ．，１３（３）（１９７４）、４１１～４１６頁にあって、特に、４１３頁参照）。即ち、従来では、例えば、発光素子用途の積層構造体を構成するに利用できるのは、基板表面の面指数と同一の面指数をもって成長したリン化硼素（ＢＰ）結晶層であった（庄野　克房著、「半導体技術（上）」（（財）東京大学出版会、１９９２年６月２５日発行９刷、７７頁及び９９頁参照）。

【０００６】また、リン化硼素（ＢＰ）については従来から様々な禁止帯幅が報告されている。例えば、Ｂ．Ｓｔｏｎｅらは多結晶ＢＰ膜から約６エレクトロンボルト（ｅＶ）の室温禁止帯幅を得ている（Ｐｈｙｓ．Ｒｅｖ．Ｌｅｔｔ．，Ｖｏｌ．４、Ｎｏ．６（１９６０）、２８２～２８４頁照）。また、Ｍａｎｃａに依れば、４．２ｅＶの禁止帯幅が提示されている（Ｊ．Ｐｈｙｓ．Ｃｈｅｍ．Ｓｏｌｉｄｓ，２０（１９６１）、２６８．参照）。また、リン化硼素の禁止帯幅は約２ｅＶであるとされている（①ＲＣＡ Ｒｅｖｉｅｗ，２５（１９６４）、１５９～１６７頁、及び②Ｚ．ａｎｏｒｇ．ａｌｌｇ．ｃｈｅｍ．，３４９（１９６７）、１５１～１５７頁参照）。現状では、リン化硼素（ＢＰ）の室温での禁止帯幅は約２ｅＶであるとして通用している（寺本　巖著、「半導体デバイス概論」（（株）培風館、１９９５年３月３０日発行初版、２８頁参照）。このため、ＬＥＤ用途の積層構造体を構成するに用いられるリン化硼素（ＢＰ）系混晶の半導体特性は、ＢＰの室温禁止帯幅を２ｅＶとして設計されている（特開平２－２７５６８２号及び特開平１０－２４７７６０号各公報参照）。

【０００７】約２ｅＶのリン化硼素（ＢＰ）を用いて、より高い禁止帯幅のＢＰ系混晶体を形成する技術も開示されている。例えば、アンドープ（ｕｎｄｏｐｅ）の窒化アルミニウム・ガリウム混晶（$Ga_{0.5}Al_{0.5}N$）薄層（層厚＝１ｎｍ）とリン化硼素（ＢＰ）薄層（層厚＝１ｎｍ）との超格子構造から２．７ｅＶの禁止帯幅を得

ている（特開平１０－２４７７４５号公報参照）。また、$Ga_{0.5}Al_{0.5}N$薄層（層厚＝１．３ｎｍ）とリン化硼素（ＢＰ）薄層（層厚＝０．７ｎｍ）との超格子構造から３．０ｅＶの禁止帯幅を得ている（特開平２－２８８３７１号公報参照）。或いは、リン化硼素（ＢＰ）を用いて、多元混晶とすることにより高い禁止帯幅のリン化硼素系混晶が得られている（上記の特開平２－２８８３７１号参照）。例えば、$Ga_{0.3}Al_{0.3}B_{0.4}N_{0.6}P_{0.4}$５元混晶として禁止帯幅を３ｅＶとする半導体層を得ている（上記の特開平２－２８８３７１号参照）。また例えば、$Ga_{0.25}Al_{0.25}B_{0.50}N_{0.60}P_{0.40}$５元混晶として禁止帯幅を２．７ｅＶとする半導体層を得ている（上記の特開平２－２８８３７１号参照）。

【０００８】

【発明が解決しようとする課題】上記の従来の技術が教示する様に、立方晶の単結晶を基板とした際に、基板と同一の面指数を有する単結晶のリン化硼素（ＢＰ）系半導体層を得ることができる温度範囲は極めて狭い。これでは、リン化硼素（ＢＰ）系半導体層を備えた積層構造体を簡便に且つ安定して形成することはできない。単結晶のリン化硼素層を帰結できる温度範囲は、リン化硼素（格子定数≒４．５４Å）の（１１１）結晶面間の面間隔（≒３．２１Å）との差異を小とする六方晶（ｈｅｘａｇｏｎａｌ）炭化珪素（ａ軸格子定数≒３．０８Å）を基板とすれば拡幅できるとされる（上記の「応用物理」、第４５巻、８９４頁参照）。単結晶のリン化硼素層が得られる温度は１０５０℃～１１５０℃となり、範囲は１００℃に拡幅できると報告されている（Ｊ．Ａｐｐｌ．Ｐｈｙｓ．，４２（１）（１９７１）、４２０～４２４頁参照）。

【０００９】また、リン化硼素層の面指数は、六方晶基板の（０００１）に対し、（１１１）となっている（上記のＪ．Ａｐｐｌ．Ｐｈｙｓ．，４２（１９７１）参照）。単量体のリン化硼素（ｂｏｒｏｎ　ｍｏｎｏｐｈｏｓｐｈｉｄｅ）は、立方硫化亜鉛鉱型（ｓｐｈａｒｅｌｉｔｅ）（上記の「半導体結合論」、１４～１５頁参照）の結晶であり、［１１０］方向に明瞭な劈開性を有する。上記の六方晶炭化珪素は明瞭な劈開性を呈し無い上に、面指数を（１１１）とする結晶層が積層したリン化硼素結晶層では劈開は容易ではない。従って、例えば、劈開面を共振面として利用するレーザダイオードを簡便に構成するに至らない。

【００１０】また、従来技術においては、ＢＰ系半導体層は禁止帯幅を約２ｅＶと低くするＢＰを母体材料として構成しているため、例えば、短波長の発光を透過するに充分な高い禁止幅を備えたＢＰ系混晶層を得るに至らなかった。一例を挙げれば、禁止帯幅を２．０ｅＶとするＢＰとＧａＰ（禁止帯幅≒２．３ｅＶ）とからは、禁止帯幅を最大でも約２．３ｅＶとする$B_XGa_{1-X}P$（$0 \leq X \leq 1$）混晶層が形成される過ぎない欠点があった。これでは、例えば、青紫色等の短波長発光が吸収されてしまうため、この様な低い禁止帯幅のリン化硼素系半導体備えた積層構造体からは、例えば、外部への発光の取出し効率に優れる高輝度のＬＥＤがもたらされない問題が生じていた。

【００１１】一方、禁止帯幅を約２ｅＶとするリン化硼素（ＢＰ）を用いてより高い禁止帯幅の半導体層を得るための従来技術では、数ｎｍ程度の極薄膜を周期的に交互に積層させて超格子構造としなければならず、極薄膜の層厚並びに組成を安定して制御するために煩雑で冗長な成膜操作を必要とする。また、超格子構造を形成するための特殊な成膜装置も要求されている（上記の特開平２－２８８３７１号参照）。更に、元来、禁止帯幅の小さなリン化硼素（ＢＰ）を用いて、例えば、５元（５元素）混晶を形成し、より高い禁止帯幅のリン化硼素（ＢＰ）系混晶層を得る従来技術では、混晶の構成元素の組成を安定に維持することは困難である。混晶の形成において、構成元素の数を増して多元混晶である程、安定な成膜は困難となるのは既に、周知である（上記の「半導体デバイス概論」、２４頁参照）。安定して形成でき、実用となっているのは砒化アルミニウム・ガリウム（$Al_XGa_{1-X}As$：$0 \leq X \leq 1$）３元混晶やリン化アルミニウム・ガリウム・インジウム（$(Al_XGa_{1-X})_YIn_{1-Y}P$：$0 \leq X \leq 1$、$0 \leq Y \leq 1$）４元混晶である（上記の「半導体デバイス概論」、２４頁参照）。

【００１２】本発明は上記の従来技術の問題点を克服すべくなされたもので、（イ）従来に無く広い温度範囲で良質の結晶層を得ることを可能と成し、（ロ）基板表面の面指数に依存せずに一定の面指数の結晶面からなり、尚且つ（ハ）その面指数が明瞭な劈開を呈する方向に合致する様に形成されたリン化硼素系半導体層から積層構造体を構成するための技術を提示する。また、（イ）及至（ハ）項に記載の特徴を有するリン化硼素系半導体層を具備した積層構造体を形成するに優位となる製造方法を提供する。更に、その積層構造体から作製した発光特性に優れる発光素子、並びにそれを用いたランプ（ｌａｍｐ）及び光源を提供することを趣旨としている。

【００１３】

【課題を解決するための手段】即ち、本発明は、単結晶の基板上に積層したリン化硼素系半導体層を備えた積層構造体であって、次の（１）乃至（６）項に記載の特徴を備えた積層構造体である。

（１）単結晶基板と、該単結晶基板の表面に設けられた非晶質または多結晶のリン化硼素系半導体からなる緩衝層と、該緩衝層上に設けられた、単結晶基板の表面に平行な表面の面指数を｛１１０｝とする結晶面が積層されてなるリン化硼素系半導体結晶層（｛１１０｝－リン化硼素系半導体結晶層という。）とを具備することを特徴とする積層構造体。

（２）｛１１０｝－リン化硼素系半導体結晶層が、面指

数を｛１００｝とする立方晶の単結晶基板の表面上に設けられていることを特徴とする前記（１）に記載の積層構造体。

（３）｛１１０｝－リン化硼素系半導体結晶層が、面指数を｛１１１｝とする立方晶の単結晶基板の表面上に設けられていることを特徴とする前記（１）に記載の積層構造体。

（４）単結晶基板上に設けた緩衝層が、面指数を｛１１０｝以外とする結晶面を含む多結晶のリン化硼素系半導体から構成されていることを特徴とする前記（１）乃至（３）の何れか１項に記載の積層構造体。

（５）単結晶基板上に設けた緩衝層が、面指数を｛１／Ｈ，１／Ｋ，１／Ｌ｝（Ｈ，Ｋ，及びＬは何れも正の整数）とする結晶面を含む多結晶のリン化硼素系半導体から構成されていることを特徴とする前記（４）に記載の積層構造体。

（６）｛１１０｝－リン化硼素系半導体結晶層が、室温での禁止帯幅を３．０±０．２エレクトロンボルト（ｅＶ）とする単量体のリン化硼素（ｂｏｒｏｎ　ｍｏｎｏｐｈｏｓｐｈｉｄｅ）を含む材料から構成されていることを特徴とする前記（１）乃至（５）の何れか１項に記載の積層構造体。

【００１４】また本発明は、次の（７）乃至（１２）項に記載の積層構造体の製造方法である。

（７）単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする前記（１）乃至（６）の何れか１項に記載の積層構造体の製造方法。

（８）表面を｛１００｝結晶面とする単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする前記（７）に記載の積層構造体の製造方法。

（９）表面を｛１１１｝結晶面とする単結晶基板上に、非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、該緩衝層上に、７５０℃以上１２００℃以下の温度範囲で、｛１１０｝－リン化硼素系半導体結晶層を形成することを特徴とする前記（７）に記載の積層構造体の製造方法。

（１０）非晶質または多結晶のリン化硼素系半導体からなる緩衝層を、｛１１０｝－リン化硼素系半導体結晶層よりも低温で形成することを特徴とする前記（７）乃至（９）の何れか１項に記載の積層構造体の製造方法。

（１１）非晶質または多結晶のリン化硼素系半導体からなる緩衝層を、２５０℃以上７００℃以下の温度で形成することを特徴とする前記（７）乃至（１０）の何れか１項に記載の積層構造体の製造方法。

（１２）２５０℃以上７００℃以下の温度で非晶質または多結晶のリン化硼素系半導体からなる緩衝層を形成した後、より高温で緩衝層に熱処理を施して、面指数を｛１／Ｈ，１／Ｋ，１／Ｌ｝（Ｈ，Ｋ，及びＬは何れも正の整数）とする結晶面を有する多結晶のリン化硼素系半導体からなる緩衝層を形成することを特徴とする前記（７）乃至（１１）の何れか１項に記載の積層構造体の製造方法。

【００１５】また本発明は、次の（１３）乃至（１７）項に記載の発光素子である。

（１３）｛１１０｝－リン化硼素系半導体結晶層からなる緩衝層を具備する前記（１）乃至（６）の何れか１項に記載の積層構造体を用いた発光素子。

（１４）｛１１０｝－リン化硼素系半導体結晶層からなる障壁層を具備する前記（１）乃至（６）の何れか１項に記載の積層構造体を用いた発光素子。

（１５）｛１１０｝－リン化硼素系半導体結晶層からなる電流阻止（狭窄）層を具備する前記（１）乃至（６）の何れか１項に記載の積層構造体を用いた発光素子。

（１６）｛１１０｝－リン化硼素系半導体結晶層からなる電極コンタクト層を具備する前記（１）乃至（６）の何れか１項に記載の積層構造体を用いた発光素子。

（１７）少なくとも一部が｛１１０｝－リン化硼素系半導体結晶層からなる半導体多層膜反射鏡を具備する前記（１）乃至（６）の何れか１項に記載の積層構造体を用いた発光素子

【００１６】また本発明は、（１８）前記（１３）乃至（１７）の何れか１項に記載の発光素子を用いたランプ。

（１９）前記（１８）に記載のランプを用いた光源。である。

【００１７】

【発明の実施の形態】本発明の第１の実施形態として、導電性のｎ形またはｐ形シリコンを基板として積層構造体を構成する例が挙げられる。加えて、ｐ形或いはｎ形リン化ガリウム（ＧａＰ）または砒化ガリウム（ＧａＡｓ）或いはリン化硼素（ＢＰ）（①Ｊ．Ｅｌｅｃｔｒｏｃｈｅｍ．Ｓｏｃ．，１２０（１９７３）、ｐ．ｐ．８０２～８０６．、及び②米国特許５，０４２，０４３号公報参照）等のＩＩＩ－Ｖ族化合物半導体単結晶を基板として利用して構成する。導電性の結晶材料を基板とすれば、基板の電気的導通性に依り、裏面に正負、何れかの極性のオーミック（Ｏｈｍｉｃ）電極を敷設できる。従って、導電性結晶基板は、サファイア等を絶縁性基板とした場合に於ける積層構造体の一部を除去し、導電性の構成層表面を露呈した上で電極を形成するといった煩雑な工程（特開平１０－３２１９０７号公報参照）を不要となし、簡便に発光素子を構成する利便な技術手段を与える。特に、抵抗率を１０ミリオーム（ｍΩ）以下とする低比抵抗の導電性単結晶基板は、順方向電圧（所

圧、Ｖｆ）を低く抑えたＬＥＤをもたらすに有効である。

【００１８】また、本発明の第１の実施形態に於ける最大の特徴は、非晶質或いは多結晶のリン化硼素系半導体からなる緩衝層を、基板と積層構造体の一構成層たる｛１１０｝−リン化硼素系半導体結晶層との中間に配置することにある。緩衝層は、例えば、一般式$B_{\alpha}Al_{\beta}Ga_{\gamma}In_{1-\alpha-\beta-\gamma}P_{1-\delta}As_{\delta}$（$0<\alpha\leq1$、$0\leq\beta<1$、$0\leq\gamma<1$、$0<\alpha+\beta+\gamma\leq1$、$0\leq\delta<1$）で表記されるリン化硼素系半導体から構成できる。また、例えば、一般式$B_{\alpha}Al_{\beta}Ga_{\gamma}In_{1-\alpha-\beta-\gamma}P_{1-\delta}N_{\delta}$（$0<\alpha\leq1$、$0\leq\beta<1$、$0\leq\gamma<1$、$0<\alpha+\beta+\gamma\leq1$、$0<\delta<1$）で表記される窒素（Ｎ）を含むリン化硼素系半導体から構成できる。好ましくは、構成元素数が少なく、簡便に構成できる２元結晶或いは３元混晶から構成する。例えば、単量体リン化硼素（ＢＰ）、リン化アルミニウム・硼素混晶（$B_{\alpha}Al_{\beta}P$：$0<\alpha\leq1$，$0\leq\beta<1$で且つ$\alpha+\beta=1$）、リン化硼素・ガリウム混晶（$B_{\alpha}Ga_{\delta}P$：$0<\alpha\leq1$、$0\leq\delta<1$で且つ$\alpha+\delta=1$）、或いはリン化硼素・インジウム混晶（$B_{\alpha}In_{1-\alpha}P$：$0<\alpha\leq1$）などから構成する。非晶質或いは多結晶からなる緩衝層は、基板と｛１１０｝−リン化硼素系半導体結晶層との格子不整合性を緩和して、ミスフィット（ｍｉｓｆｉｔ）転位等の結晶欠陥密度が小さく結晶性に優れる｛１１０｝−リン化硼素系半導体結晶層をもたらす作用を有する。

【００１９】非晶質或いは多結晶の緩衝層は、基板を構成する単結晶材料に格子整合するリン化硼素系半導体からも構成できる（特開２０００−２２２１１号公報参照）。例えば、リン化硼素・ガリウム（$B_{0.32}Ga_{0.68}P$：格子定数≒５．４５０Å）や砒化硼素・ガリウム（$B_{0.23}Ga_{0.77}As$：格子定数≒５．４５０Å）等からはＧａＰ単結晶（格子定数≒５．４５０Å）基板と格子整合を果たす緩衝層を構成できる（上記の特開２０００−２２２１１号参照）。また、シリコン（格子定数≒５．４３１Å）基板に格子整合する緩衝層の構成材料例として$B_{0.02}Ga_{0.98}P$がある。基板に格子整合する緩衝層は、上記の作用に加えて、基板からの積層構造体の構成層の剥離を防止するに特に効果がある。また、リン化硼素系半導体からなる緩衝層は、上層としてリン化硼素系半導体層を設けるに際し、均等な成長を促す「成長核」を提供するため、平坦で連続性のある上層をもたらす作用を発揮できる。特に、リン化硼素系半導体層をその構成元素を含まない単結晶基板、例えばシリコン基板上に設ける場合、リン化硼素系半導体からなる緩衝層は上層を構成する元素の吸着サイト（ｓｉｔｅ）の役目を果たし、均等な成長を促進させるに有効に作用する。

【００２０】リン化硼素系半導体からなる緩衝層は、ＭＯＣＶＤ法（Ｉｎｓｔ．Ｐｈｙｓ．Ｃｏｎｆ．Ｓｅｒ．，Ｎｏ．１２９（ＩＯＰ Ｐｕｂｌｉｓｈｉｎｇ Ｌｔｄ．，１９９３）、１５７〜１６２頁参照）、分子線エピタキシャル（ＭＢＥ）法（Ｊ．Ｓｏｌｉｄ Ｓｔａｔｅ Ｃｈｅｍ．，１３３（１９９７）、２６９〜２７２頁参照）、ハライド（ｈａｌｉｄｅ）法（①「日本結晶成長学会誌」、Ｖｏｌ．２４、Ｎｏ．２（１９９７）、１５０頁及び②Ｊ．Ａｐｐｌ．Ｐｈｙｓ．，４２（１）（１９７１）、４２０〜４２４頁参照）、及びハイドライド（ｈｙｄｒｉｄｅ）法等の気相成長手段に依り形成できる。特に、ＭＯＣＶＤ手段は、構成元素の原料は全て気体であり、その気体原料の流量或いは供給流量比率を調整すれば、簡便に所望の伝導型の結晶層が得られるため（Ｊ．Ｃｒｙｓｔａｌ Ｇｒｏｗｔｈ、２４／２５（１９７４）、１９３〜１９６頁参照）、リン化硼素系半導体層の形成に利便である。ＭＯＣＶＤ法に利用できる気相反応系としてトリエチル硼素（$(C_2H_5)_3B$）／ボラン（BH_3）またはジボラン（B_2H_6）／ホスフィン（PH_3）またはターシャリィブチル（ｔｅｒｔ．−ｂｕｔｈｙｌ）ホスフィン等の有機リン化合物反応系を例示できる（Ｊｐｎ．Ｊ．Ａｐｐｌ．Ｐｈｙｓ．，１３（３）（１９７４）、４１１〜４１６頁参照）。

【００２１】特に、非晶質或いは多結晶からなる緩衝層は、上記の気相成長手段において、成膜温度を２５０℃〜７００℃とすることで形成できる。低い成膜温度とする程、非晶質を主体とするリン化硼素系半導体からなる緩衝層が得られ易くなる。２５０℃以下では成膜用原料の分解が充分に進行しないため、成膜は不安定で不都合である。約４５０℃を越える成膜温度では、多結晶を主体とするリン化硼素系半導体からなる緩衝層が帰結され易くなる。７００℃を越える温度では充分な格子不整合の緩和効果を発揮できかねる良質の結晶層が得られ易くなり不都合である。緩衝層が非晶質層或いは多結晶層であることは、一般的なＸ線回折法や電子線回折法等に依り解析できる。基板材料との格子の整合性の有無に拘わらず、緩衝層の層厚は大凡、１ｎｍ以上で１００ｎｍ以下、更に好ましくは、２ｎｍ以上で５０ｎｍ以下とするのが望ましい。適当な層厚のリン化硼素系半導体を緩衝層として配置して、格子歪を緩和する作用を活かせば、緩衝層上に単結晶基板の表面に平行な表面の面指数を｛１１０｝とする結晶面が積層されてなる単結晶のリン化硼素系半導体層を積層させられる。

【００２２】本発明の云う面指数とは、結晶面を表すための指標であるミラー（Ｍｉｌｌｅｒ）指数を指す（Ｃ．Ｗ．バン著、「化学結晶学」（昭和４５年６月１５日、（株）培風館発行初版、２１〜２２頁参照）。例えば、面指数を｛１１０｝とする結晶面とは、（１１０）、（−１１０）、（−１−１０）、（１−１０）等の（１１０）に等価な結晶面の総称である。また、例えば、面指数を｛１１１｝とする結晶表面とは、（１１１）或いは（−１−１−１）等の（１１１）に等価な結

晶面から構成される表面のことである。立方晶閃亜鉛鉱型の単結晶基板上に形成した緩衝層を利用すれば、単結晶基板表面を構成する結晶面の面指数に拘わらず、一定の面指数を有するリン化硼素系半導体結晶層をもたらすことができる。例えば、ＭＯＣＶＤ手段に依り、形成温度を７５０℃以上で１２００℃以下として本発明に係わる上記の緩衝層を利用すれば、その上に単結晶基板の表面に平行な表面の面指数を｛１１０｝とする結晶面が積層されてなるリン化硼素系半導体結晶層（｛１１０｝－リン化硼素系半導体結晶層）を形成できる。図４に基板表面を構成する結晶面に平行にリン化硼素系半導体結晶層の｛１１０｝結晶面が配列している模様を模式的に示す。即ち、本発明に係わる非晶質または多結晶からなるリン化硼素系半導体からなる緩衝層は、基板をなす単結晶の結晶場の影響を弱小として面指数が一定の結晶面の積層からなるリン化硼素系半導体結晶層をもたらす作用を有する。また、併せて、本発明に係わる緩衝層は、良質のリン化硼素系半導体結晶層を帰結する温度範囲を従来に無く広い４５０℃の範囲に拡幅する作用を有する。１２００℃を越える高温では、リン化硼素系半導体を構成するリン（Ｐ）の揮散に因る孔（ｐｉｔ）が顕著に発生するため、平滑な表面のリン化硼素系半導体結晶層を安定して帰結しないため不適である。

【００２３】本発明の第２の実施形態では、表面の結晶面の面指数を｛１００｝とする立方晶基板、例えば、閃亜鉛鉱型の｛１００｝－単結晶基板上に｛１１０｝－リン化硼素系半導体結晶層を積層して積層構造体を構成する。｛１００｝－単結晶基板の表面に平行に｛１１０｝－リン化硼素系半導体結晶層が積層されていると、Ｘ線回折図形（パターン）には一般に、｛１００｝－単結晶基板に起因する回折と、併せて、｛１１０｝－リン化硼素系半導体結晶層からの回折が出現する。これより、本発明に係わる単結晶基板とリン化硼素系半導体結晶層との結晶面についての相互関係が達成されているか否かが知れる。図５に一例として、｛１００｝－Ｓｉ単結晶基板上に、３５０℃で形成したリン化硼素緩衝層を介して、８００℃で形成した単量体のリン化硼素結晶層についてのＸ線回折図形（パターン）を掲げる。｛１００｝－Ｓｉ単結晶基板に由来する｛４００｝－Ｓｉ結晶面からのブラッグ（Ｂｒａｇｇ）回折ピーク（回折角度２θ≒６９．１°）に加え、ＢＰ結晶層からの｛２２０｝回折ピーク（回折角度２θ≒５７．６°）が現れている。これより、｛１００｝－単結晶基板の表面に平行に｛１１０｝－リン化硼素系半導体層が積層されていることが分かる。この様な構成の積層構造体からは、例えば、劈開面を共振端面とする直方体状のレーザダイオードを簡便に構成できる利点がある。

【００２４】例えば、閃亜鉛鉱型の｛１１１｝結晶面表面に於ける構成原子の占有率は、｛１００｝結晶面よりも大である。このため、｛１１１｝－単結晶基板では、リン化硼素系半導体からなる緩衝層を構成するリン（Ｐ）または硼素（Ｂ）の基板内部への拡散、浸透を抑制して、層厚の制御された緩衝層を安定してもたらすに効果を奏する。従って、本発明の第３の実施形態では、面指数を｛１１１｝とする立方晶基板、例えば、閃亜鉛鉱型の｛１１１｝－単結晶基板上に｛１１０｝－リン化硼素系半導体層を積層させることとして積層構造体を構成する。図６に一例として、｛１１１｝－Ｓｉ単結晶基板上に、３５０℃で形成したリン化硼素緩衝層を介して、９００℃で形成した単量体のリン化硼素結晶層についてのＸ線回折図形（パターン）を掲げる。｛１１１｝－Ｓｉ単結晶基板に由来する｛２２２｝回折ピーク（回折角度２θ≒５８．８°）に加え、ＢＰ結晶層からの｛２２０｝回折ピーク（回折角度２θ≒５７．６°）が現れている。これより、｛１１１｝－単結晶基板の表面に平行に｛１１０｝－リン化硼素系半導体結晶層が積層されているのが分かる。この様な結晶面の配向関係は電子線回折法に依っても調査できる。

【００２５】｛１００｝或いは｛１１１｝の何れの面指数を有する単結晶基板かに依らずにもたらされる｛１１０｝－リン化硼素系半導体結晶層は、短波長光を放射するに好都合な窒化ガリウム（ＧａＮ）系半導体からなる発光層（特公昭５５－３８３４号公報参照）を積層するに優位な下地層として作用する。立方硫化亜鉛鉱型（ｓｐｈａｒｅｌｉｔｅ）（フィッリプス著、「半導体結合論」（（株）吉岡書店、１９８５年７月２５日発行、第３刷）、１４～１５頁参照）の結晶である単量体リン化硼素（ｂｏｒｏｎ　ｍｏｎｏｐｈｏｓｐｈｉｄｅ：ＢＰ）は、立方晶（ｃｕｂｉｃ）の窒化ガリウム（ｃ－ＧａＮ：格子定数＝４．５１０Å）と略同一の４．５３８Åの格子定数を有する（上記の「半導体デバイス概論」、２８頁参照）。更に、ＢＰの｛１１０｝結晶面の間隔は約３．２０９Åであり、六方晶（ｈｅｘａｇｏｎａｌ）ＧａＮ（ｈ－ＧａＮ）のａ軸格子定数である３．１８０Åと略同等であるため、ＧａＮ系半導体との格子の整合性が良好である。従って、｛１１０｝－リン化硼素系半導体層上には、格子のミスマッチに起因する結晶欠陥の少ない結晶性に優れるＧａＮ系発光層を積層できる利点がある。

【００２６】本発明の第４の実施形態に於ける構成上の特徴は、単結晶基板上に設ける非晶質または多結晶から構成する緩衝層を、特に、面指数を｛１１０｝以外とする結晶面を含む多結晶のリン化硼素系半導体層から構成したことにある。例えば、｛１１１｝、｛３１１｝、または｛１００｝等の結晶面を含む多結晶層から構成する。この様なミラー指数の結晶面を緩衝層の内部に発生させることに依り、基板を構成する単結晶と積層構造体構成層との格子不整合性を緩和し、且つ、積層欠陥や反位相粒界を吸収して結晶欠陥密度の少ない積層構造体構成層をもたらす作用を有する。多結晶緩衝層の内部で

の、｛１１０｝結晶面とそれ以外の上記の様な結晶面との含有比率は、例えば、一般のＸ線回折法で取得できる｛１１０｝回折ピークとの強度比から求められる。望ましい構成は、｛１１０｝回折ピークの強度に対して、例えば、｛１１１｝回折ピークの強度比を約１／５、より好ましいのは約１／１０、即ち、｛１１１｝結晶面の含有率が｛１１０｝結晶面の１／５～１／１０とした場合である。更に好ましいのは、｛１１０｝結晶面に起因するＸ線回折ピーク強度に対し、その他の結晶面からの回折ピークの強度の合計の比率が約１／５～１／１０であることである。

【００２７】また、本発明の第５の実施形態では、単結晶基板上に設ける非晶質または多結晶から構成する緩衝層を、面指数を｛１／Ｈ，１／Ｋ，１／Ｌ｝（Ｈ，Ｋ，及びＬは何れも正の整数）とする、限定された面指数の結晶面を含む多結晶のリン化硼素系半導体層から構成する。面指数を｛１／Ｈ，１／Ｋ，１／Ｌ｝（Ｈ，Ｋ，及びＬは何れも整数）とする結晶面とは、例えば、｛１１１｝、｛－１－１－１｝、｛３１１｝、｛－３１１｝等の結晶面である。これらの限定された結晶面は、基板を構成する単結晶と積層構造体構成層との格子歪を緩和すると共に、特に、積層欠陥等の面欠陥等を吸収する作用を発揮して結晶性に優れる積層構造体構成層をもたらすに貢献できる。本発明に係わる薄層の緩衝層については、例えば、透過型電子顕微鏡（ＴＥＭ）を使用する断面ＴＥＭ技法並びに電子線回折技法等に依って、層内部の結晶形態、組織及び結晶面の構成を把握できる。

【００２８】上記の第５の実施形態に係わる限定された結晶面を含むリン化硼素系半導体からなる緩衝層は、２５０℃以上７００℃以下の温度で一旦単結晶基板上に一旦、層を形成した後、形成温度よりも高温で熱処理すれば形成できる。例えば、リン化ガリウム（ＧａＰ）単結晶基板の表面上に、例えば、４００℃で一旦、層厚を約５ｎｍとする非晶質のリン化硼素・ガリウム（$B_{0.5}Ga_{0.5}P$）緩衝層を形成する。その後、例えば、８５０℃に昇温し、同温度にて例えば２０分間に亘り保持すれば、上記の限定された結晶面を含むリン化硼素系半導体からなる緩衝層を構成できる。緩衝層に約７５０℃～８５０℃の比較的低温で熱処理を施すと、｛１１０｝結晶面と｛１１１｝結晶面を主体として含む多結晶緩衝層が得られる。約１０００℃の高温では、｛１１１｝結晶面に加えて、｛３１１｝結晶面を含む多結晶緩衝層が形成され易くなる。緩衝層を１２００℃を越える高温で熱処理するのは、リン（Ｐ）の揮散に因る、緩衝層表面の平坦性を劣化させるので好ましくない。また、１２００℃を越える高温で緩衝層に例えば、アニール（ａｎｎｅａｌ）を施すと、組成式B_6Pや$B_{13}P_2$で表記されるリン化硼素多量体が発生し（Ｊ．Ａｍ．Ｃｅｒａｍｉｃ Ｓｏｃ．，４７（１）（１９６４）、４４～４６頁参照）、均質な緩衝層の形成が阻害されるため好ましくはない。

【００２９】本発明の第６の実施形態では、室温での禁止帯幅（ｂａｎｄ ｇａｐ）を３．０±０．２ｅＶとするリン化硼素（ＢＰ）を含む材料から｛１１０｝－リン化硼素系半導体結晶層を構成し、それを用いて積層構造体を形成する。高い禁止帯幅を有する単量体のＢＰを用いれば、従来に無く高い禁止帯幅を有するリン化硼素系半導体層を構成することができる。例えば、禁止帯幅を２．０ｅＶとする従来のＢＰでは、２．０ｅＶ以上で、最高でもＧａＰの禁止帯幅に相当する２．３ｅＶと低く、且つ取り得る範囲の狭いリン化硼素・ガリウム（$B_XGa_{1-X}P$：０≦Ｘ≦１）混晶がもたらされるのみであった。これに対し、本発明に依れば、２．３ｅＶ以上で３．０±０．２ｅＶの広範囲に亘る、高い禁止帯幅の$B_XGa_{1-X}P$（０≦Ｘ≦１）混晶をもたらすことができる。高い禁止帯幅のリン化硼素系半導体層は、例えば、単一（Ｓｉｎｇｌｅ Ｈｅｔｅｒｏ：ＳＨ）または二重（Ｄｏｕｂｌｅ Ｈｅｔｅｒｏ：ＤＨ）接合型発光部から放射される発光を透過するに好都合に作用する発光透過用窓層等として利用できる。

【００３０】室温での禁止帯幅を３．０±０．２ｅＶ以下とするリン化硼素（ＢＰ）は、特に、積層の際の成長速度と原料の供給比率の双方を規程された範囲内に設定することにより形成できる（特願２００１－１５８２８２号明細書参照）。成長速度は、好ましくは、毎分２０Å以上で３００Å以下とする（上記の特願２００１－１５８２８２号参照）。成長速度を２０Å／ｍｉｎ未満の遅い速度とすると、成長層表面からのリン（Ｐ）構成元素或いはその化合物が脱離、揮発が充分に抑止されず、成膜が果たせない場合がある。３００Å／ｍｉｎを越える速い成長速度に設定すると、得られる禁止帯幅の値が不安定となり好ましくはない。また、成長速度を徒に速くすると多結晶の結晶層となり易い傾向にあり、良質の結晶層を得るには不都合となる。

【００３１】また、成長速度と併せて、原料の供給比率を好ましくは１５以上で６０以下の範囲に規定する。ＢＰ層を形成する場合にあって、原料の供給比率とは、成長反応系への硼素（Ｂ）原料の供給量に対するリン（Ｐ）原料の供給量の比率である。また、ＢＰ系混晶を形成する場合にあっては、硼素（Ｂ）を含むＩＩＩ族構成元素原料の合計の供給量に対する、リン（Ｐ）を含むＶ族構成元素原料の合計の供給量の比率である。リン化硼素・インジウム（$B_{\alpha}In_{1-\alpha}P$：０＜α≦１）混晶を形成する場合を例にすれば、成長反応系に供給するガリウム（Ｇａ）原料とインジウム（Ｉｎ）原料の総量に対する、リン（Ｐ）原料の供給量の比率である。即ち、所謂、Ｖ／ＩＩＩ比率である。Ｖ／ＩＩＩ比率を１５未満と小とすると、成長層表面が乱雑となり望ましくはない。また、ＩＩＩ／Ｖ比率を６０を越えて極端に大とすると、化学量論的に観てリン（Ｐ）が富裕な状態である

成長層が形成され易くなる。過剰なリン（Ｐ）は、結晶格子で硼素（Ｂ）が占有すべき位置に入り込み、ドナー（ｄｏｎｏｒ）として働くとされる（庄野　克房著、「超ＬＳＩ時代の半導体技術１００集〔５〕」（（株）オーム社、昭和５９年５月１日発行、電子雑誌エレクトロニクス第２９巻第５号（昭和５９年５月号）付録、１２１頁参照）。化学量論的組成がリン（Ｐ）の富裕側に移行してしまえば、低抵抗のｐ形結晶層の形成に支障を来すので不都合である。

【００３２】本発明の第１３乃至第１７の実施形態では、｛１１０｝－リン化硼素系半導体結晶層を各種の機能層として具備する積層構造体から発光素子を構成する。例えば、本発明に係わる、単結晶基板上に、非晶質または多結晶の緩衝層を介して形成した｛１１０｝－リン化硼素系半導体結晶層は、結晶性に優れる結晶層となる。このため、ＳＨまたはＤＨ接合構造からなる発光部を設けるにあたり、良質の発光部構成層をもたらせる下地（被堆積）層としての緩衝層として有用に利用できる。従って、第１３の実施形態では、本発明に係わる｛１１０｝－リン化硼素系半導体結晶層を緩衝層として形成することにより、良質な結晶層から構成できることとなった発光部を備えた積層構造体から発光素子を構成できる。例えば、｛１１１｝－シリコン基板上に多結晶のリン化硼素（ＢＰ）緩衝層を介して設けた｛１１０｝－リン化硼素系半導体結晶層を緩衝層とし、その上に例えば窒化リン化ガリウム（$GaN_{1-X}P_X$：０≦Ｘ≦１）を発光層とするｐｎ接合型ＤＨ構造の発光部を備えた積層構造体からＬＥＤを構成する。

【００３３】本発明の第１４の実施形態では、｛１１０｝－リン化硼素系半導体結晶層を障壁層として備えた積層構造体から発光素子を構成する。特に、高禁止帯幅の｛１１０｝－リン化硼素半導体結晶層からは、発光層との障壁の差異を充分に大とする障壁層を提供できる利点がある。例えば、単量体ＢＰ（禁止帯幅≒３．０ｅＶ、格子定数≒４．５３８Å）からは、立方晶$GaN_{0.97}P_{0.03}$（禁止帯幅≒２．７ｅＶ、格子定数≒４．５３８Å）発光層に対し、禁止帯幅の差異を０．３ｅＶとする高障壁のクラッド（ｃｌａｄ）層を構成できる。また、高い禁止帯幅の｛１１０｝－リン化硼素系半導体結晶層を、例えば、発光を外部視野方向に透過できる窓を兼用するクラッド層として利用すれば、高輝度のＬＥＤを構成できる利点がある。

【００３４】リン化硼素（ＢＰ）はイオン結合性が小さく、ｐ形及びｎ形の導電性の結晶層が得られ易いため、ｐｎ接合構造を簡便に構成できる。このｐｎ接合を例えば、発光部上に設ければ、本発明の第１５の実施形態に係わる、｛１１０｝－リン化硼素系半導体結晶層を電流阻止層または電流狭窄層として備えた発光素子を構成できる。更に具体的には、｛１１０｝－リン化硼素系半導体結晶層からなるｐｎ接合を、ＬＥＤ動作電流を流通させるための台座（ｐａｄ）電極の直下に配置して構成する。台座電極の射影領域にあたる例えば、シングルヘテロ（ＳＨ）またはダブルヘテロ（ＤＨ）接合構造発光部をなすクラッド（ｃｌａｄ）層表面上に配置する。この様に配置すれば、台座電極を介して供給される素子動作電流の台座電極の直下の領域（所謂、発光を外部へ容易に取り出せない台座電極の射影領域）への流通が阻止され、逆に開放発光領域へ優先的に流通させられる。このため、高輝度のＬＥＤを構成するに寄与できる。

【００３５】また、例えば、酸素（Ｏ）を添加してなした｛１１０｝－リン化硼素系半導体結晶層は、電流阻止層としてレーザダイオード（ＬＤ）を構成するために利用できる。例えば、ＤＨ構造発光部上に電流阻止層を一旦、積層させた後、それを帯状（ストライプ状）に削除し、発光部の表層部を露出させる。その後、残置した電流阻止層と露出させた発光部の表面とを被覆する様に導電性半導体層を積層する。この様な構成とすれば、高密度の動作電流を開口部の直下の発光部に集中して注入できるため、電流狭窄型のＬＤを好都合に構成できる。

【００３６】本発明の第１６の実施形態では、｛１１０｝－リン化硼素系半導体結晶層を電極コンタクト層として備えた積層構造体から発光素子を構成することとする。リン化硼素（ＢＰ）系結晶は、立方晶閃亜鉛鉱型結晶のため、価電子帯の縮帯構造（生駒　俊明、生駒　英明共著、「化合物半導体の基礎物性入門」（１９９１年９月１０日、（株）培風館発行初版、１４～１７頁参照））と、低イオン結合性故に（上記の「半導体結合論」、４９～５１頁参照）、特に、ｐ形で低抵抗の導電層を簡易に構成できる利点を有する。従って、低い接触抵抗のオーミック性電極を形成するに貢献できる。このため、順方向電圧（所謂、Ｖｆ）の低いＬＥＤ、或いは閾値電圧（所謂、Ｖｔｈ）の低いＬＤがもたらされる。ｐ形の｛１１０｝－リン化硼素系半導体結晶層からなるコンタクト層上に設けるｐ形オーミック電極は、例えば、金・亜鉛（Ａｕ・Ｚｎ）合金等から構成できる。また、ｎ形の｛１１０｝－リン化硼素系半導体結晶層からなるコンタクト層上には、金・ゲルマニウム（Ａｕ・Ｇｅ）合金、金・インジウム（Ａｕ・Ｉｎ）合金、又は金・錫（Ａｕ・Ｓｎ）合金などの金合金等からｎ形オーミック電極を形成できる。

【００３７】また、単結晶基板の表面に平行に配列した、表面の平坦性に優れる｛１１０｝－リン化硼素系半導体結晶層を利用すれば、発光を外部視野方向に反射できる反射鏡を都合良く構成できる（「面発光レーザ」（（株）オーム社、１９９０年９月２５日発行第１版第１刷、１０５～１１７頁参照）。この様な反射鏡は屈折率を異にする異種または異なる組成の半導体薄膜を相互に周期的に重層させて構成する（上記の「面発光レーザ」、１１８～１１９頁参照）。この周期的重層構造を屈折率の相違を大とする半導体薄膜から構成すると、周

期数（重層サイクル数）を少なくして反射率を高くする多層膜反射鏡を効率的に形成できる。尚且つ、多層膜反射鏡を相互に格子整合する半導体薄膜から構成すれば、反射率の高い高性能の半導体多層膜反射鏡を構成できる。例えば、リン化硼素（屈折率≒３．１）と略格子整合の関係にある窒化ガリウム（屈折率≒２．５：上記の「半導体デバイス概論」、２８頁参照）とを交互に重層させた構造から反射鏡を構成できる。従って、｛１１０｝－リン化硼素系半導体結晶層を半導体多層膜反射鏡の一方の構成層として備えている積層構造体からは、外部への発光の取り出し効率に優れる、高輝度のＬＥＤを提供できる。本発明の第１７の実施形態では、屈折率を大きく相違し、且つ略格子整合、更に望ましくは格子整合の関係にある半導体薄膜の交互重層構造から構成した、広帯域に亘り高い反射率をもたらす反射鏡を備え、該反射鏡の構成層の少なくとも一部が｛１１０｝－リン化硼素系半導体結晶層からなる半導体多層膜反射鏡を具備する積層構造体から発光素子を構成する。

【００３８】上記の本発明の第１３乃至第１７の実施形態に係わる発光素子からは、高輝度のランプを構成できる。例えば、本発明の第１８の実施形態のランプは、次の工程をもって構成できる。図７に例示する如く、基板１１上に本発明に係わる｛１１０｝－リン化硼素系半導体結晶層からなる電流阻止層１２を備えたＬＥＤ１０を、台座１５上の銀（Ａｇ）或いはアルミニウム（Ａｌ）等の金属を鍍金した金属製碗体１６の中央部に導電性の接合材で固定する。これより、基板１１の底面に設けた一極性の電極１４を台座１５に付属する一端子１７に電気的に接続させる。また、ヘテロ接合構造上に設置した電極１３を台座１５に付属する他の一方の端子１８に結線する。一般的な半導体封止用のエポキシ樹脂１９で碗体１６を囲繞する様に封止すればランプを構成できる。また、本発明に依れば、約２００μｍ～約３００μｍ角の小型ＬＥＤも形成でき、従って、特に、設置容積を小とする表示器等として好適な小型の発光ダイオードランプを構成できる。

【００３９】また、ＬＥＤチップ或いは樹脂封止されたダイオードランプを集合させれば、本発明に係わる光源を構成できる。例えば、複数のＬＥＤを電気的に並列に接続させて、例えば、定電圧駆動型の光源を構成できる。また、電気的に直列にダイオードランプを接続して定電流型の光源を構成できる。これらのＬＥＤを利用する光源は、従来の白熱型のランプ光源とは異なり、点灯によりさほど放熱を伴わないため、冷光源として特に有用に利用できる。例えば、冷凍食品の展示用光源として利用できる。また、例えば、屋外表示器、交通信号を提示するための信号器、自動車用途等の方向指示器或いは照明機器等に好適に用いられる光源を構成できる。

【００４０】

【作用】本発明に記載の基板表面の結晶面に平行に、｛１１０｝結晶面を配列してなる｛１１０｝－リン化硼素系半導体結晶層は、発光素子にあって緩衝層として機能できるため、結晶性に優れる構成層からなる発光部をもたらす作用を有する。また、障壁層として機能できるため、放射再結合を起こすキャリアを「閉じ込める」作用を有する。また、電流阻止層として機能できるため、素子駆動電流を外部へ開口された発光領域に優先的に流通させる作用を発揮する。また、電極コンタクト層として機能できるため、低接触抵抗のオーミック性電極をもたらす作用を発揮する。また、半導体多層膜反射鏡として機能できるため、発光を効率的に外部視野方向に反射する作用を有する。

【００４１】本発明に記載の非晶質または多結晶からなるリン化硼素系半導体から構成される緩衝層は、結晶性に優れる、単結晶基板の表面に平行な｛１１０｝結晶面を有するリン化硼素系半導体結晶層をもたらす作用を有する。特に、｛１１０｝結晶面以外に、｛１／Ｈ，１／Ｋ，１／Ｌ｝（Ｈ，Ｋ，Ｌは正の整数）結晶面を含んでなる多結晶からなるリン化硼素系半導体からなる緩衝層は、格子歪、結晶欠陥等を吸収して、良質の｛１１０｝－リン化硼素系半導体結晶層をもたらす作用を有する。

【００４２】本発明に記載の、室温で禁止帯幅を３．０±０．２ｅＶとする高い禁止帯幅のリン化硼素（ＢＰ）を含む材料から構成されているリン化硼素系半導体層は、従来に無い高い禁止帯幅を有する発光透過（窓）層として優位に作用する。

【００４３】

【実施例】（実施例１）アズーグローン（ａｓ－ｇｒｏｗｎ）状態では非晶質を主体としてなるリン化硼素（ＢＰ）系半導体層を具備した積層構造体から発光ダイオード（ＬＥＤ）を構成する場合を例にして本発明を具体的に説明する。本実施例１に係わるＬＥＤ１Ａの断面模式図を図１に示す。

【００４４】本実施例１に係わる発光素子用途の積層構造体１Ｂは、硼素（Ｂ）ドープｐ形（１１１）－Ｓｉ単結晶を基板１０１として構成した。基板１０１上には、トリエチル硼素（$(C_2H_5)_3B$）／ホスフィン（PH_3）／水素（H_2）系常圧ＭＯＣＶＤ法により、３５０℃で成長させた非晶質を主体とするリン化硼素緩衝層１０２を堆積した。緩衝層１０２の層厚は約５ｎｍとした。

【００４５】緩衝層１０２の表面には、上記のＭＯＣＶＤ気相成長手段を利用して、８５０℃で、Ｓｉ基板の表面の（１１１）結晶面に平行に配列した表面が｛１１０｝結晶面からなる単量体の｛１１０｝－リン化硼素（ＢＰ）からなるｐ形下部クラッド層１０３を積層した。ｐ形の不純物はマグネシウム（Ｍｇ）とし、そのドーピング原料にはビス－シクロペンタジエニルマグネシウム（ｂｉｓ－$(C_5H_4)_2Mg$）を用いた。下部クラッド層１０３のキャリア濃度は約8×10^{18}ｃｍ$^{-3}$とし

た。層厚は８００ｎｍとした。本発明に係わる結晶組織を有する緩衝層１０２を下地層としたため、下部クラッド層１０３は亀裂（ｃｒａｃｋ）の無いリン化硼素連続層から構成できた。また、緩衝層１０２よりも高温で下部クラッド層１０３の形成を終了した後では、緩衝層１０２は多結晶層に変化していた。

【００４６】ｐ形｛１１０｝－ＢＰ下部クラッド層１０３上には、リン化硼素（ＢＰ；格子定数＝４．５３８Å）に格子整合する立方晶のｎ形$GaN_{0.97}P_{0.03}$層（格子定数＝４．５３８Å）から構成した発光層１０４を積層させた。発光層１０４をなす$GaN_{0.97}P_{0.03}$層の結晶表面は、下部クラッド層１０３をなすＢＰ層表面の｛１１０｝結晶面に平行に配列した、｛１１０｝結晶面から主に構成されたものとなった。発光層１０４の形成時に、ｎ形のドーパントとして珪素（Ｓｉ）を添加することにより、発光層１０４のキャリア濃度は約1×10^{17}ｃｍ$^{-3}$に調整した。発光層１０４の層厚は約１２０ｎｍとした。

【００４７】ｎ形$GaN_{0.97}P_{0.03}$発光層１０４の表面上には、上記のＭＯＣＶＤ反応系によりｎ形のＢＰ層からなる上部クラッド層１０５を積層した。上部クラッド層１０５は、発光層１０４の表面に対して垂直方向に｛１１０｝結晶面を重層してなる｛１１０｝結晶面を有する単量体のリン化硼素から構成した。ｎ形のドーパントは珪素（Ｓｉ）として、キャリア濃度は約8×10^{16}ｃｍ$^{-3}$に調整した。層厚は８０ｎｍとした。８５０℃と成長温度を同一として成膜したｐ形｛１１０｝－ＢＰ下部クラッド層１０３、ｎ形$GaN_{0.97}P_{0.03}$発光層１０４、及びｎ形｛１１０｝－ＢＰ上部クラッド層１０５からｐｎ接合型ダブルヘテロ（ＤＨ）構造の発光部を形成した。

【００４８】上部クラッド層１０５上には、円形の台座電極１０６を配置した。台座電極１０８は金・ゲルマニウム（Ａｕ９５質量％・Ｇｅ５質量％）真空蒸着膜から構成した。台座電極１０６の直径は１２０μｍとした。また、ｐ形Ｓｉ基板１０１の裏面の略全面には、ｐ形オーミック電極１０７を配置してＬＥＤ１Ａを構成した。ｐ形オーミック電極１０７はアルミニウム（Ａｌ）真空蒸着膜から構成した。Ｓｉ単結晶基板１０１を［２１１］方向に平行及び垂直な方向に裁断して、一辺を約３００μｍとする正方形のＬＥＤチップ１Ａとした。

【００４９】台座電極１０６とｐ形オーミック電極１０７との間に順方向に２０ミリアンペア（ｍＡ）の動作電流を通流した際の発光中心波長は約４１５ｎｍとなった。一般的な積分球を利用して測定されるチップ（ｃｈｉｐ）状態での輝度は約８ミリカンデラ（ｍｃｄ）となり、高発光強度のリン化硼素系ＬＥＤ１Ａが提供された。Ｉ－Ｖ特性から求めた順方向電圧（所謂、Vf）は約３．６Ｖ（順方向電流＝２０ｍＡ）となった。また、逆方向電圧は約８Ｖ（逆方向電流＝１０μＡ）であり、高耐圧のＬＥＤが提供された。

【００５０】（実施例２）特定の面指数の結晶面を内包する多結晶のリン化硼素（ＢＰ）系半導体層を具備した積層構造体から発光ダイオード（ＬＥＤ）を構成した。本実施例２では、上記の実施例１と同様の図１に示す構造の積層構造体からＬＥＤを構成した。

【００５１】本実施例２では、リン（Ｐ）ドープｎ形（１００）２°オフ（ｏｆｆ）Ｓｉ単結晶を基板として利用した。同基板上には、トリエチル硼素（$(C_2H_5)_3B$）／トリメチルガリウム（$(CH_3)_3Ga$）／ホスフィン（PH_3）／水素（H_2）系減圧ＭＯＣＶＤ法により、５５０℃で成長させた多結晶を主体とするアンドープでｎ形のリン化硼素・ガリウム混晶層を堆積した。ＭＯＣＶＤ成長時の圧力は約6×10^4パスカル（圧力単位：Ｐａ）に設定した。層厚は約８ｎｍとした。リン化硼素・ガリウム混晶の硼素（Ｂ）組成比は、Ｓｉ単結晶（格子定数≒５．４３１Å）基板に格子整合する０．０２（$B_{0.02}Ga_{0.98}P$：格子定数≒５．４３１Å）に設定した。

【００５２】リン化硼素・ガリウム（$B_{0.02}Ga_{0.98}P$）層の堆積を終えた後、同層をホスフィン（PH_3）とアルゴン（Ａｒ）との混合雰囲気（$PH_3$２．５体積％＋Ａｒ９７．５体積％）中で、７５０℃に昇温した。７５０℃の一定温度で１５分間、保持した。この熱処理により、$B_{0.02}Ga_{0.98}P$層を｛１１１｝結晶面及び｛３１１｝結晶面を含む多結晶の緩衝層となした。

【００５３】次に、緩衝層の温度を上記のリン化合物を含む不活性ガス雰囲気内で９００℃に上昇させた。緩衝層の表面には、上記のＭＯＣＶＤ気相成長手段により、Ｓｉ基板の表面の（１００）結晶面に平行に配列した表面が｛１１０｝結晶面からなるリン化硼素・ガリウム（$B_{0.98}Ga_{0.02}P$）からなるｎ形下部クラッド層を積層した。ｎ形｛１１０｝－$B_{0.98}Ga_{0.02}P$層は、９００℃、成長時の圧力約8×10^4Ｐａの条件下で形成した。ｎ形不純物は珪素（Ｓｉ）とし、そのドーピング原料にはジシラン（Si_2H_6）を体積百万分率にして約５０ｖｏｌ．ｐｐｍ含む水素（H_2）との混合ガスを用いた。下部クラッド層のキャリア濃度は約2×10^{18}ｃｍ$^{-3}$とした。層厚は８００ｎｍとした。本発明に係わる結晶組織を有する多結晶の緩衝層を下地層としたため、下部クラッド層は亀裂（ｃｒａｃｋ）の無いリン化硼素・ガリウムの連続膜から構成できた。また、本実施例２に依れば、｛２２０｝結晶面からのＸ線回折ピークの強度は、実施例１の下部クラッド層を構成する｛１１０｝－リン化硼素層よりも約１．２倍高いものとなった。また、ｎ形｛１１０｝－$B_{0.98}Ga_{0.02}P$層の室温での禁止帯幅は、成長速度を毎分約２５ｎｍとし、Ｖ／ＩＩＩ比率（＝PH_3／（$(CH_3)_3Ga$＋$(C_2H_5)_3B$）供給比率）を４５として成膜したため、約３．０ｅＶとなった。

【００５４】ｎ形｛１１０｝－$B_{0.98}Ga_{0.02}P$下部クラッド層上には、$B_{0.98}Ga_{0.02}P$（格子定数≒４．５５７Å）に格子整合する立方晶のｎ形$GaN_{0.95}P_{0.05}$層（格子定数＝４．５５７Å）から構成した発光層を積層させた。発光層の$GaN_{0.95}P_{0.05}$層の結晶表面も、下部クラッド層をなす$B_{0.98}Ga_{0.02}P$層表面の｛１１０｝結晶面に平行に配列した、｛１１０｝結晶面から主に構成されるものとなった。発光層の形成時には、ｎ形のドーパントとして珪素（Ｓｉ）を添加して、発光層のキャリア濃度を約３×10^{17}ｃｍ$^{-3}$に調整した。また、発光層の層厚は約１００ｎｍとした。

【００５５】ｎ形$GaN_{0.95}P_{0.05}$発光層の表面上には、上記のＭＯＣＶＤ反応系によりｐ形の$B_{0.98}Ga_{0.02}P$層からなる上部クラッド層を積層した。上部クラッド層は、発光層の表面に対して垂直方向に｛１１０｝結晶面を重層してなる｛１１０｝結晶面を有する結晶層から構成した。ｐ形のドーパントはマグネシウム（Ｍｇ）として、キャリア濃度は約４×10^{18}ｃｍ$^{-3}$に調整した。層厚は２００ｎｍとした。また、ｐ形｛１１０｝－$B_{0.98}Ga_{0.02}P$層の室温での禁止帯幅は、成長速度を毎分約２５ｎｍとし、Ｖ／ＩＩＩ比率（PH_3／（$(CH_3)_3Ga$＋$(C_2H_5)_3B$）供給比率）を４５として成膜したため、約３．０ｅＶとなった。このため、$B_{0.98}Ga_{0.02}P$上部クラッド層は、発光を外部視野方向に透過するための発光透過窓層としても利用した。９００℃と成長温度を同一として成膜したｎ形｛１１０｝－$B_{0.98}Ga_{0.02}P$下部クラッド層、ｎ形$GaN_{0.95}P_{0.05}$発光層、及びｐ形｛１１０｝－$B_{0.98}Ga_{0.02}P$上部クラッド層からｐｎ接合型ダブルヘテロ（ＤＨ）構造の発光部を形成した。

【００５６】上部クラッド層上には、円形のオーミック性台座電極を配置した。台座電極は金・亜鉛（Ａｕ９５質量％・Ｚｎ５質量％）真空蒸着膜から構成した。台座電極の直径は１１０μｍとした。また、ｎ形Ｓｉ基板の裏面の略全面には、ｎ形オーミック電極を配置してＬＥＤを構成した。ｎ形オーミック電極はアルミニウム（Ａｌ）・アンチモン（Ｓｂ）合金の真空蒸着膜から構成した。上部クラッド層をなす｛１１０｝－$B_{0.98}Ga_{0.02}P$結晶層の［１１０］結晶方向に平行に劈開して、一辺を約３００μｍとする正方形のチップ（ｃｈｉｐ）となした。

【００５７】台座電極とｎ形オーミック電極の間に順方向に２０ミリアンペア（ｍＡ）の動作電流を通流した際の発光中心波長は約４７０ｎｍとなった。一般的な積分球を利用して測定されるチップ（ｃｈｉｐ）状態での輝度は約８ミリカンデラ（ｍｃｄ）となり、高発光強度のＬＥＤが提供された。Ｉ－Ｖ特性から求めた順方向電圧（所謂、Ｖｆ）は約３．５Ｖ（順方向電流＝２０ｍＡ）となった。また、逆方向電圧は約８Ｖ（逆方向電流＝１０μＡ）であり、高耐圧のＬＥＤが提供された。

【００５８】（実施例３）｛１１０｝結晶面を有するリン化硼素（ＢＰ）半導体層を構成層とする半導体多層膜反射鏡と、｛１１０｝結晶面を有する単量体のＢＰ層からなる緩衝層とを具備した積層構造体からＬＥＤを構成した。本実施例３のＬＥＤ３Ａの断面構造を図２に模式的に示す。実施例１に記載のＬＥＤ１Ａと同一の構成要素については、図２で同一の符号を付す。

【００５９】本実施例３では、硫黄（Ｓ）ドープｎ形（１００）２°オフ（ｏｆｆ）リン化ガリウム（ＧａＰ）単結晶を基板１０１として利用した。基板１０１上には、トリエチル硼素（$(C_2H_5)_3B$）／トリメチルガリウム（$(CH_3)_3Ga$）／ホスフィン（PH_3）／水素（H_2）系減圧ＭＯＣＶＤ法により、４５０℃で成長させた多結晶を主体とするアンドープでｎ形のリン化硼素・ガリウム（$B_XGa_{1-X}P$：０≦Ｘ≦１）緩衝層１０２を堆積した。ＭＯＣＶＤ成長時の圧力は約６×10^4パスカル（圧力単位：Ｐａ）に設定した。層厚は約１２ｎｍとした。リン化硼素・ガリウム混晶（$B_XGa_{1-X}P$）の硼素（Ｂ）組成比（＝Ｘ）は、基板１０１のＧａＰ単結晶（格子定数≒５．４５０Å）と単量体ＢＰ（格子定数≒４．５３８Å）との中間の格子定数を有する０．５０（$B_{0.50}Ga_{0.50}P$：格子定数≒４．９９４Å）に設定した。

【００６０】リン化硼素・ガリウム（$B_{0.50}Ga_{0.50}P$）多結晶緩衝層１０２上には、表面が｛１１０｝結晶面からなる珪素（Ｓｉ）ドープｎ形リン化硼素（ＢＰ）緩衝層（キャリア濃度≒１×10^{18}ｃｍ$^{-3}$、層厚≒９５０ｎｍ）１０８を積層させた。｛１１０｝－単量体ＢＰ緩衝層１０８は、上記の減圧ＭＯＣＶＤ手段により、８５０℃で形成した。

【００６１】単結晶緩衝層１０８上には、ＢＰ薄膜１０９ａと、Ｓｉドープｎ形窒化ガリウム（ＧａＮ）単結晶薄膜１０９ｂとから構成した半導体多層膜反射鏡１０９を設けた。反射鏡１０９を構成するＢＰ薄膜１０９ａとＧａＮ薄膜１０９ｂの膜厚は何れも約５２ｎｍとした。また、キャリア濃度は何れの薄膜１０９ａ、１０９ｂも約１×10^{18}ｃｍ$^{-3}$とした。反射鏡１０９は、｛１１０｝－ＢＰ緩衝層１０３の表面上に、ＧａＮ薄膜１０９ｂと｛１１０｝－ＢＰ薄膜１０９ａとを接合させた単位積層構造を５周期に重層させた積層構造から構成した。

【００６２】半導体多層膜反射鏡１０９の表層をなす｛１１０｝－ＢＰ薄膜１０９ａ上には、上記のＭＯＣＶＤ手段に依り、８５０℃で単量体の｛１１０｝－ＢＰ結晶層からなる障壁（下部クラッド）層１０３を積層した。下部クラッド層１０３は、特に、成長速度を毎分１０ｎｍとし、また、Ｖ／ＩＩＩ（＝PH_3／$(CH_3)_3Ga$）比率を３５に設定して形成して、室温の禁止帯幅を約３．１ｅＶとする単量体の｛１１０｝－ＢＰ結晶層から構成した。Ｓｉドープｎ形下部クラッド層１０３のキャリア濃度は約２×10^{18}ｃｍ$^{-3}$とし、層厚は約４０

０ｎｍとした。

【００６３】ｎ形｛１１０｝－ＢＰ下部クラッド層１０３上には、単量体ＢＰ（格子定数≒４．５３８Å）に格子整合する立方晶のｎ形$Ga_{0.94}In_{0.06}N$層（格子定数≒４．５３８Å）から構成した発光層１０４を積層させた。発光層１０４の$Ga_{0.94}In_{0.06}N$層の結晶表面も、下部クラッド層をなす｛１１０｝－ＢＰ層表面の｛１１０｝結晶面に平行に配列した、｛１１０｝結晶面から主に構成されるものとなった。発光層１０４の形成時には、ｎ形のドーパントとしてＳｉを添加して、キャリア濃度を約$3\times10^{17}cm^{-3}$調整した。また、発光層１０４の層厚は約１００ｎｍとした。

【００６４】ｎ形$Ga_{0.94}In_{0.06}N$発光層１０４の表面上には、上記のＭＯＣＶＤ反応系に依り、８５０℃でｐ形の単量体ＢＰ層からなる上部クラッド層１０５を積層した。上部クラッド層１０５は、発光層の表面に対して垂直方向に｛１１０｝結晶面を重層してなる｛１１０｝－結晶層から構成した。ｐ形のドーパントはマグネシウム（Ｍｇ）として、キャリア濃度は約$3\times10^{18}cm^{-3}$に調整した。層厚は３００ｎｍとした。また、ｐ形｛１１０｝－ＢＰ層の室温での禁止帯幅は、成長速度を毎分約４０ｎｍとし、Ｖ／ＩＩＩ比率（＝PH_3／（$(CH_3)_3Ga$＋$(C_2H_5)_3B$）供給比率）を４５として成膜したため、室温での禁止帯幅は約３．１ｅＶとなった。このため、｛１１０｝－ＢＰ上部クラッド層１０５は、発光を外部視野方向に透過するための発光透過窓層としても利用できた。８５０℃と成長温度を同一として成膜したｎ形｛１１０｝－ＢＰ下部クラッド層１０３、ｎ形$Ga_{0.94}In_{0.06}N$発光層１０４、及びｐ形｛１１０｝－ＢＰ上部クラッド層１０５からｐｎ接合型ダブルヘテロ（ＤＨ）構造の発光部を形成した。

【００６５】｛１１０｝－ＢＰ上部クラッド層１０５上には、円形のオーミック性台座電極を配置した。台座電極は金・亜鉛（Ａｕ９５質量％・Ｚｎ５質量％）真空蒸着膜から構成した。台座電極の直径は１３０μｍとした。また、ｎ形ＧａＰ基板の裏面の略全面には、ｎ形オーミック電極を配置してＬＥＤ３Ａを構成した。ｎ形オーミック電極は金（Ａｕ）・ゲルマニウム（Ｇｅ）合金の真空蒸着膜から構成した。上部クラッド層１０５をなす｛１１０｝－ＢＰ結晶の［１１０］結晶方向に平行に劈開して、一辺を約３５０μｍとする正方形のチップ（ｃｈｉｐ）となした。

【００６６】台座電極とｎ型オーミック電極の間に順方向に２０ミリアンペア（ｍＡ）の動作電流を通流した際の発光中心波長は約４７０ｎｍとなった。一般的な積分球を利用して測定されるチップ（ｃｈｉｐ）状態での輝度は約８ミリカンデラ（ｍｃｄ）となり、高発光強度のＬＥＤが提供された。Ｉ－Ｖ特性から求めた順方向電圧（所謂、Ｖｆ）は約３．５Ｖ（順方向電流＝２０ｍＡ）となった。また、逆方向電圧は約８Ｖ（逆方向電流＝１０μＡ）であり、高耐圧のＬＥＤが提供された。

【００６７】（実施例４）｛１１０｝結晶面からなるリン化硼素（ＢＰ）系半導体層を電流狭窄層として、また、電極コンタクト層として具備するレーザダイオード（ＬＤ）用途の積層構造体を構成した。本実施例４の積層構造体４Ｂの断面構造を図３に模式的に示す。第１または実施例３に記載のＬＥＤ１Ａ、３Ａと同一の構成要素については、図３で同一の符号を付す。

【００６８】積層構造体４Ｂは、アンチモン（Ｓｂ）ドープｎ形（１００）２°オフ（ｏｆｆ）珪素（Ｓｉ）単結晶を基板１０１として構成した。基板１０１上には、トリエチル硼素（$(C_2H_5)_3B$）／トリメチルガリウム（$(CH_3)_3Ga$）／ホスフィン（PH_3）／水素（H_2）系常圧（略大気圧）ＭＯＣＶＤ法により、３５０℃で成長させた非晶質を主体とするアンドープでｎ形のリン化硼素・ガリウム（$B_XGa_{1-X}P$：０≦Ｘ≦１）緩衝層１０２を堆積した。層厚は約１５ｎｍとした。リン化硼素・ガリウム混晶（$B_XGa_{1-X}P$）の硼素（Ｂ）組成比（＝Ｘ）は、基板１０１のＳｉ単結晶（格子定数≒５．４３１Å）と格子整合する０．０２（$B_{0.02}Ga_{0.98}P$：格子定数≒５．４３１Å）に設定した。

【００６９】非晶質のリン化硼素・ガリウム（$B_{0.02}Ga_{0.98}P$）緩衝層１０２の堆積を終えた後、緩衝層１０２をホスフィン（PH_3）と窒素（N_2）との混合雰囲気（$PH_3$３．０体積％＋Ａｒ９７．０体積％）中で、８５０℃に昇温した。８５０℃の一定温度で２０分間、保持し、非晶質の$B_{0.02}Ga_{0.98}P$層を｛１１１｝結晶面及び｛３１１｝結晶面を含む多結晶の緩衝層１０２となした。

【００７０】リン化硼素・ガリウム（$B_{0.02}Ga_{0.98}P$）多結晶緩衝層１０２上には、｛１１０｝結晶面を有する珪素（Ｓｉ）ドープｎ形リン化硼素（ＢＰ）結晶緩衝層（キャリア濃度≒$1\times10^{18}cm^{-3}$、層厚≒６５０ｎｍ）１０８を積層させた。｛１１０｝－単量体ＢＰ緩衝層１０８は、上記の常圧ＭＯＣＶＤ手段により、８５０℃で形成した。

【００７１】緩衝層１０８上には、上記のＭＯＣＶＤ手段に依り、８５０℃で単量体の｛１１０｝－ＢＰ結晶層からなる障壁（下部クラッド）層１０３を積層した。下部クラッド層１０３は、特に、成長速度を毎分２５ｎｍとし、また、Ｖ／ＩＩＩ（PH_3／$(CH_3)_3Ga$）比率を５０に設定して形成して、室温の禁止帯幅を約３．１ｅＶとする単量体の｛１１０｝－ＢＰ結晶層から構成した。Ｓｉドープｎ形下部クラッド層１０３のキャリア濃度は約$2\times10^{18}cm^{-3}$とし、層厚は約５００ｎｍとした。

【００７２】ｎ形｛１１０｝－ＢＰ下部クラッド層１０３上には、単量体ＢＰ（格子定数≒４．５３８Å）に格子整合する立方晶のｎ形$GaN_{0.97}P_{0.03}$層（格子定数≒４．５３８Å）から構成した発光層１０４を積層させ

た。発光層１０４の$GaN_{0.97}P_{0.03}$層の結晶表面も、下部クラッド層をなす｛１１０｝－ＢＰ層表面の｛１１０｝結晶面に平行に配列した、｛１１０｝結晶面から主に構成されるものとなった。発光層１０４の形成時には、ｎ形のドーパントとしてＳｉを添加して、キャリア濃度を約$1\times10^{17}cm^{-3}$に調整した。また、発光層１０４の層厚は約９５ｎｍとした。

【００７３】ｎ形$GaN_{0.97}P_{0.03}$発光層１０４の表面上には、上記のＭＯＣＶＤ反応系に依り、８５０℃でｐ形の単量体ＢＰ層からなる上部クラッド層１０５を積層した。上部クラッド層１０５は、発光層の表面に対して垂直方向に｛１１０｝結晶面を重層してなる｛１１０｝結晶面を有する結晶層から構成した。ｐ形のドーパントはマグネシウム（Ｍｇ）として、キャリア濃度は約$2\times10^{18}cm^{-3}$に調整した。層厚は３００ｎｍとした。また、ｐ形｛１１０｝－ＢＰ層の室温での禁止帯幅は、成長速度を毎分約２５ｎｍとし、Ｖ／ＩＩＩ（＝PH_3／（$(CH_3)_3Ga$＋$(C_2H_5)_3B$））比率を５０として成膜したため、室温での禁止帯幅は約３．１ｅＶとなった。８５０℃と成長温度を同一として成膜したｎ形｛１１０｝－ＢＰ下部クラッド層１０３、ｎ形$GaN_{0.97}P_{0.03}$発光層１０４、及びｐ形｛１１０｝－ＢＰ上部クラッド層１０５からｐｎ接合型ダブルヘテロ（ＤＨ）構造の発光部を形成した。

【００７４】｛１１０｝－ＢＰ上部クラッド層１０５上には、上記のＭＯＣＶＤ手段に依り、８５０℃で酸素（Ｏ）をドーピングした高抵抗の｛１１０｝－ＢＰ結晶層を電流狭窄層１１０として積層させた。酸素添加｛１１０｝－ＢＰ結晶層は、成膜時に、酸素（O_2）を体積百万分率にして約１０ｖｏｌ．ｐｐｍ含むアルゴン（Ａｒ）との混合ガスを用いて作製した。電流狭窄層１１０内部の酸素原子濃度は一般的な２次イオン質量分析法（ＳＩＭＳ）により約3×10^{18}原子／cm^3と定量された。また、電流狭窄層１１０は、抵抗率（比抵抗）を約10^2オーム・センチメートル（Ω・ｃｍ）とする｛１１０｝－ＢＰ結晶層から構成した。層厚は約５００ｎｍとした。

【００７５】電流狭窄層１１０を形成した後、特定の領域に限定して電流狭窄層１１０をアルゴン（Ａｒ）／メタン（CH_4）／水素（H_2）系プラズマエッチング法により除去した。電流狭窄層１１０を除去した領域は、一般的なストライプ（帯状）構造型（「半導体レーザー基礎と応用－」（１９９７年１０月３０日、（株）培風館発行初版第６刷）、１０～１１頁参照）のレーザダイオード（ＬＤ）を構成するための帯状電極（図示せず）を設ける予定領域の下方の帯状領域１１１に限定した。電流狭窄層１１０を除去した帯状領域１１１には、｛１１０｝－ＢＰ結晶層からなる上部クラッド層１０５の表面を露呈させた。

【００７６】上部クラッド層１０５の表面を露出させた帯状領域１１１と、帯状領域１１１を中間に挟んで対向して残置させた電流狭窄層１１０の表面を、ｐ形の砒化リン化硼素（$BAs_{0.05}P_{0.95}$）混晶層で被覆した。｛１１０｝－$BAs_{0.05}P_{0.95}$混晶層は、（$(C_2H_5)_3B$）／アルシン（AsH_3）／水素（H_2）系常圧（略大気圧））ＭＯＣＶＤ法により、８５０℃で成長させた。オーミック性表面電極（図示せず）を形成するための電極コンタクト層１１２として利用した$BAs_{0.05}P_{0.95}$混晶層のキャリア濃度は約$2\times10^{18}cm^{-3}$とし、層厚は約１５０ｎｍとした。以上により、レーザダイオード（ＬＤ）用途の積層構造体４Ｂを構成した。

【００７７】

【発明の効果】本発明に依れば、非晶質または多結晶のリン化硼素系半導体層からなる緩衝層を介して、従来に無い広い温度範囲で形成できる、基板表面の面指数に依存せずに、明瞭な劈開を施せる｛１１０｝の一定の面指数を有するリン化硼素系半導体結晶層を利用して積層構造体を構成することとしたので、劈開により簡便に素子を構成するに好適な積層構造体を提供できる。

【００７８】本発明に依れば、特に、特定の結晶面を内包する多結晶のリン化硼素系半導体からなる緩衝層を介することにより、従来に無い広い温度範囲で形成できる、基板表面の面指数に依存せずに、明瞭な劈開を施せる｛１１０｝の一定の面指数を有するリン化硼素系半導体結晶層を備えた積層構造体を効率的に得られる。

【００７９】本発明に依れば、非晶質または多結晶のリン化硼素系半導体層からなる緩衝層を介することにより、従来に無い広い温度範囲で形成できる、基板表面の面指数に依存せずに、明瞭な劈開を施せる｛１１０｝の一定の面指数を有するリン化硼素系半導体結晶層を備えた積層構造体から発光素子を構成することとしたので、高輝度の発光素子を提供できる。

【図面の簡単な説明】

【図１】実施例１に記載のＬＥＤの断面模式図である。

【図２】実施例３に記載のＬＥＤの断面模式図である。

【図３】実施例４に記載のＬＤ用途の積層構造体の断面模式図である。

【図４】本発明に係わるリン化硼素系結晶層を構成する｛１１１｝結晶面と単結晶基板表面との配列の関係を示す結晶層の断面模式図である。

【図５】｛１００｝－Ｓｉ単結晶基板上の｛１１０｝－リン化硼素系半導体結晶層のＸ線回折スペクトル例である。

【図６】｛１１１｝－Ｓｉ単結晶基板上の｛１１０｝－リン化硼素系半導体結晶層のＸ線回折スペクトル例である。

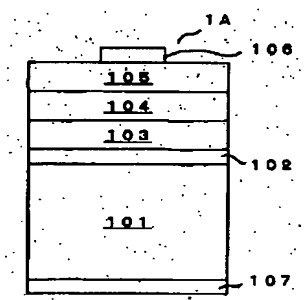
【図７】本発明に係わるランプの断面構造を例示する模式図である。

【符号の説明】

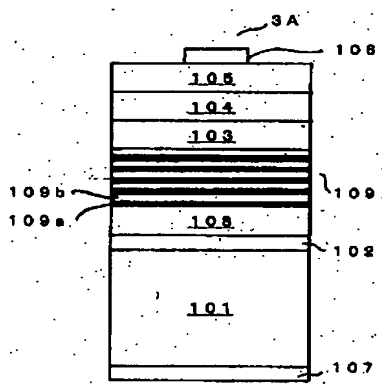
１Ａ、３Ａ、４Ａ、１０　発光素子（ＬＥＤ）

４Ｂ　レーザダイオード（ＬＤ）用途積層構造体
１１　基板
１２　リン化硼素半導体電流阻止層
１３　表面側電極
１４　基板裏面電極
１５　台座
１６　碗体
１７、１８　端子
１９　封止樹脂
１０１　単結晶基板
１０２　非晶質または多結晶緩衝層
１０３　下部クラッド層
１０４　発光層
１０５　上部クラッド層
１０６　表面電極
１０７　裏面電極
１０８　リン化硼素系半導体緩衝層
１０９　半導体多層膜反射鏡
１０９ａ　反射鏡を構成するＧａＮ薄膜
１０９ｂ　反射鏡を構成する｛１１０｝－ＢＰ薄膜
１１０　電流狭窄層
１１１　帯状領域
１１２　電極コンタクト層

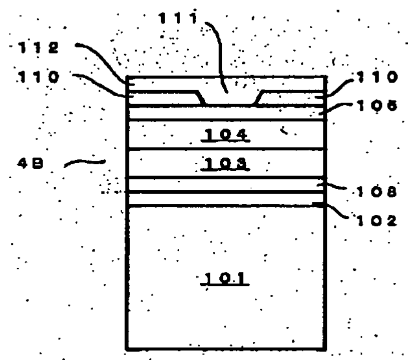
【図１】



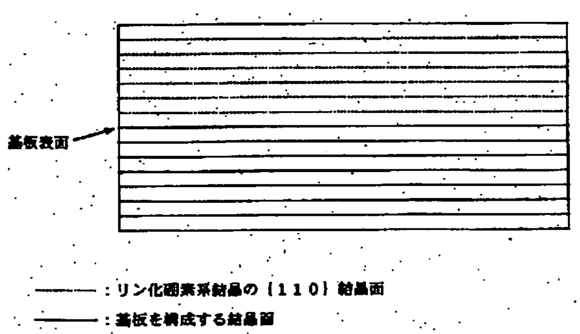
【図２】



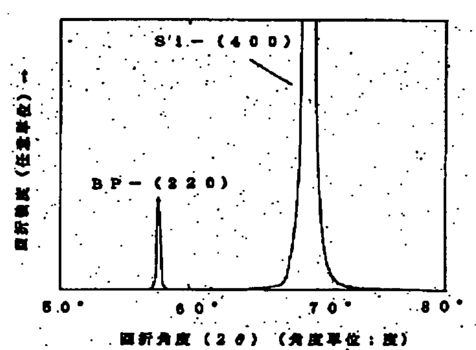
【図３】



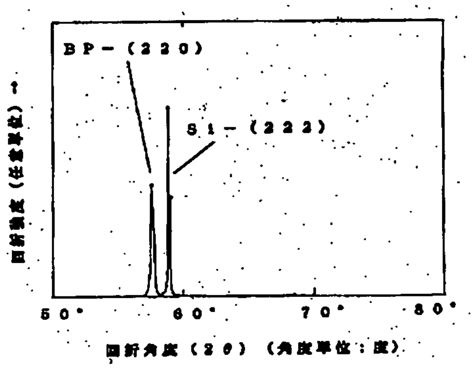
【図４】



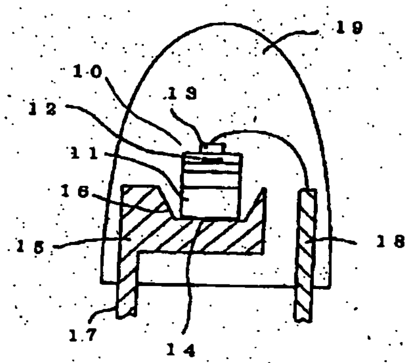
【図５】



【図６】



【図７】



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